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Dept. of Computer Science and Engineering
Washington University in St. Louis

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Michael J. Hall, Viktor Gruev, and Roger D. Chamberlain
Department of Computer Science & Engineering
Washington University in St. Louis
Email: {mhall24, vgruev, roger}@wustl.edu

***Abstract*—Magnetic tunnel junction devices represent state in the form of a magnetic field that is accessed as a resistance. Read circuits are needed to sense this state and to produce a digital logic voltage output. We designed a resistance-to-voltage read circuit for this purpose. This paper presents area, transient response, power, and jitter characterizations in a 3M2P $0.5\,\mu\mathrm{m}$ process and compares these results to a second implementation in a 5M1P $0.18\,\mu\mathrm{m}$ process. As the process scales down to smaller dimensions, area decreases, rise/fall times decrease, propagation times decrease, maximum frequency increases, power consumption decreases, and jitter decreases. We then evaluate the quality of phase measurements between read circuits for assessing clock skew in systems that use magnetic global clocking. Phase delays above $1.25\,\mathrm{ns}$ can be detected and are linear above $2\,\mathrm{ns}$.**

I. Introduction

Magnetic tunnel junction (MTJ) devices are thin-film magnetic devices that are responsive to external magnetic fields. If these devices are distributed on a chip, they can be used to sense an oscillating global magnetic field and produce local clock signals. Read circuits that can sense the transients in the magnetic field are needed to produce these clock signals.

A static RAM cell read circuit is described in [1], but the MTJ state is sampled and is not continuous. Thus it is not suitable for sensing global magnetic fields. Current conveyors, however, can be designed to perform continuous reading of the MTJ state. They are used in Magnetic RAM (MRAM) [2], [3], but not for continuous reading. Rather, the current conveyor circuit is shared amongst many MRAM cells which are intermittently read. Our intent is to have a read circuit dedicated to each MTJ.

The MTJ device, shown in Figure 1, consists of two ferromagnetic layers separated by an insulator. The top ferromagnetic layer, i.e. the free layer, allows its magnetic orientation to change in the presence of a magnetic field. The bottom ferromagnetic layer, the fixed layer, has its orientation pinned during the manufacturing process. The middle layer is a thin insulator such as MgO [4].

The magnetic orientation of the free layer in the MTJ device is set by applying an external magnetic field that exceeds the hysteresis threshold of the device. The MTJ state is determined by the magnetic orientation in the free layer relative to the fixed layer and is accessed as a resistance (R_{mtj}). A device is characterized by its resistance-area (RA) product, which can range from $10\,\Omega \cdot \mu\mathrm{m}^2$ [5] to $7.6\,\mathrm{k}\Omega \cdot \mu\mathrm{m}^2$ [2].

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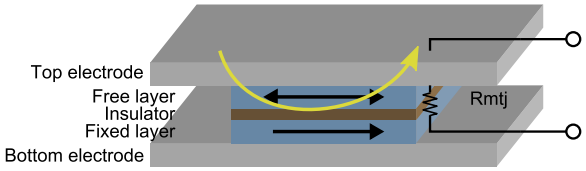

Figure 1. A magnetic tunnel junction (MTJ) device with state information encoded in the magnetic orientation of the free layer. An external magnetic field applied to the free layer sets this state and it is accessed as a resistance (R_{mtj}) between the two electrodes.

We have designed a current-conveyor-based resistance-to-voltage (R2V) read circuit based on previous work [6] for use in global clocking that performs a continuous read to sense an input resistance and produce a rail-to-rail logic voltage output.

We intend to interface the R2V read circuit with magnetic tunnel junction (MTJ) devices and to evaluate the feasibility of magnetic global clocking with these devices in a test chip. This paper presents area, transient response, power, and jitter characterizations with simulation results of an R2V read circuit in a 3 metal 2 poly (3M2P) $0.5\,\mu\mathrm{m}$ process and compares these results to a second implementation in a 5 metal 1 poly (5M1P) $0.18\,\mu\mathrm{m}$ process. We then briefly evaluate the quality of phase measurements between read circuits for measuring clock skew in systems that use magnetic global clocking.

II. Read Circuit

The R2V read circuit is shown in Figure 2. It consists of three parts: current conveyor, current comparator, and rail-to-rail output buffer. The current conveyor pins a voltage across the input resistance and produces an output current inversely proportional to the input resistance. That current is compared to a threshold current, I_{th}, by the current comparator, and then amplified rail-to-rail by the output buffer.

Current conveyor: The current conveyor circuit, formed by transistors M_{1-6}, consists of two back-to-back current mirrors; one formed by a PMOS-cascode structure and the second one by an NMOS one. It is designed to have equal currents flowing through both branches.

This circuit operates by clamping the voltage V_{mtj} to V_{bias} over the resistance R_{mtj} at the input. The current I_{mtj} that

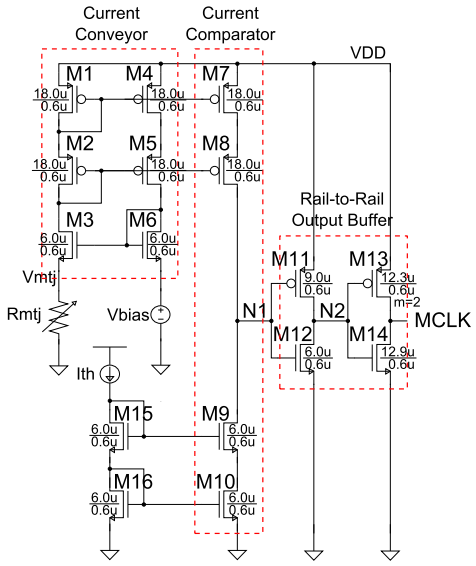

Figure 2. Resistance-to-voltage (R2V) read circuit (3M2P 0.5 μm process).

flows through M_{1-3} and R_{mtj} is $I_{mtj} = \frac{V_{bias}}{R_{mtj}}$. I_{mtj} is then mirrored to the current comparator through the current mirror formed by $M_{1,2}$ and $M_{7,8}$. All transistors operate in the saturation region satisfying the conditions $V_{ds} > V_{ds,sat}$ for NMOS and $V_{sd} > V_{sd,sat}$ for PMOS. Transistors $M_{1,2,6}$ are diode-connected and therefore always operate in saturation.

Transistors $M_{3,4,5}$ are determined by design equations and are biased such that they operate at the edge of the saturation region in order to get the smallest aspect ratio. Body and lambda effects are not considered:

$$\frac{W}{L}_3 > \frac{\frac{18V_{bias}}{K_N R_{mtj}}}{\left(V_{DD} - |V_{TP}| - max\left(|V_{TP}|, V_{TN}\right) - V_{bias}\right)^2} \quad (1)$$

$$\frac{W}{L}_{4,5} > \frac{\frac{18V_{bias}}{K_P R_{mtj}}}{\left(V_{DD} - |V_{TP}| - max\left(|V_{TP}|, V_{TN}\right) - V_{bias}\right)^2} \quad (2)$$

Here, all aspect ratios for NMOS transistors are equal ($\frac{W}{L}_3 = \frac{W}{L}_6$) and all aspect ratios for PMOS transistors are equal ($\frac{W}{L}_1 = \frac{W}{L}_2 = \frac{W}{L}_4 = \frac{W}{L}_5$). V_{DD} is the supply voltage, V_{TN} is the NMOS threshold voltage, V_{TP} is the PMOS threshold voltage, K_N is the NMOS transconductance parameter, K_P is the PMOS transconductance parameter, V_{bias} is the input bias voltage, and R_{mtj} is the input MTJ resistance.

Current comparator: The current comparator, formed by transistors M_{7-10}, compares an output current to a threshold current, I_{th}, and converts it to a logic voltage output [7]. $M_{1,2}$ current is copied and sourced by transistors $M_{7,8}$. Likewise, $M_{15,16}$ current is copied and sunk by transistors $M_{9,10}$. The output voltage V_{N1} at node $N1$ will swing depending on which current is greater. The voltage swing is determined analytically (using 1st order approximations) as

$$2\sqrt{\frac{2I_{th}}{\frac{W}{L}_{9,10} \cdot K_N}} + V_{TN} < V_{N1} < V_{DD} - 2\sqrt{\frac{2I_{mtj}}{\frac{W}{L}_{7,8} \cdot K_P}} - |V_{TP}|$$

Table I
RELEVANT PROCESS PARAMETERS

	3M2P 0.5 μm	**5M1P 0.18 μm**
V_{DD}	5.0 V	1.8 V
K_N/K_P	110/32 $\frac{\mu A}{V^2}$	342/74 $\frac{\mu A}{V^2}$
V_{TN}/V_{TP}	0.77/–0.95 V	0.5/–0.49 V

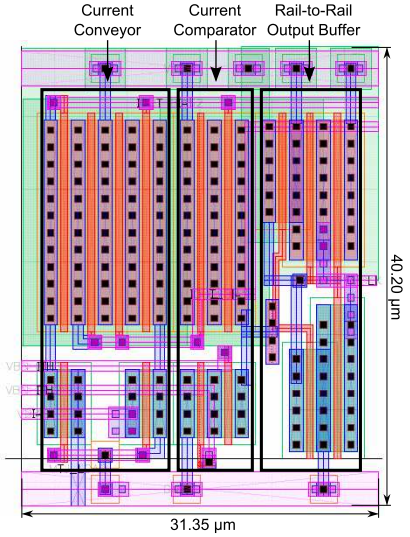

Figure 3. Layout of the R2V read circuit in the 3M2P 0.5 μm process. The sub-circuits highlighted in black boxes are (left) current conveyor, (middle) current comparator, and (right) rail-to-rail output buffer.

where I_{mtj} is the current through R_{mtj}, I_{th} is the threshold current, and $\frac{W}{L}_i$ is the aspect ratio of the i^{th} transistor.

Rail-to-Rail Output Buffer: The last stage of the read circuit is the rail-to-rail output buffer formed by transistors M_{11-14}. This buffer performs voltage amplification of the current comparator output voltage V_{N1} to get a rail-to-rail logic voltage output MCLK used to drive downstream logic. The buffer is designed to drive a 600 fF capacitive load with 1 ns rise/fall times (10-90%).

III. LAYOUT AND SIMULATION

We laid out and simulated the R2V read circuit in the 3M2P 0.5 μm process and the 5M1P 0.18 μm process to compare how circuit characteristics change at smaller process dimensions. Table I compares the relevant process parameters. The circuit is characterized in terms of area, transient response, power, and jitter in the Cadence Design Environment using Spectre simulator.

A. Area

The R2V read circuit is designed using the smallest transistors that will operate in the saturation region and still perform well. The layout of the circuit is shown in Figure 3. The dimensions of the circuit are 31.35 μm by 40.20 μm.

For the 5M1P 0.18 μm process implementation, the read circuit is redesigned with transistor aspect ratios set according to equations (1) and (2) to ensure the current conveyor transistors operate in the saturation region. The current conveyor

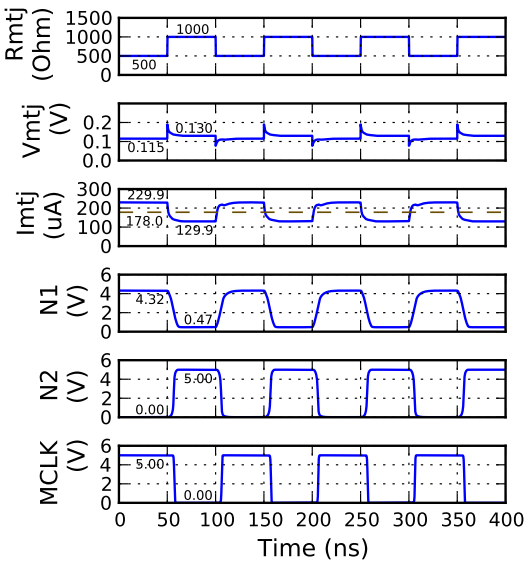

Figure 4. Transient response of the R2V read circuit at 10 MHz frequency. R_{mtj} is the input resistance, V_{mtj} is the voltage over R_{mtj}, I_{mtj} is the current through R_{mtj}, $N1$ is the current comparator output, $N2$ is the first inverter output, and $MCLK$ is the read circuit output. Threshold current, I_{th}, is indicated by the dashed line on I_{mtj}.

Table II
RISE/FALL TIMES (10-90%) AND PROPAGATION DELAY OF CIRCUIT

	3M2P 0.5 μm		**5M1P 0.18 μm**	
	t_{rise}	t_{fall}	t_{rise}	t_{fall}
N1	9.275 ns	7.767 ns	5.430 ns	5.240 ns
N2	2.702 ns	2.694 ns	0.805 ns	0.809 ns
MCLK	0.977 ns	0.964 ns	0.225 ns	0.230 ns
$t_{p,rise2fall}$	7.215 ns		4.625 ns	
$t_{p,fall2rise}$	6.691 ns		2.403 ns	

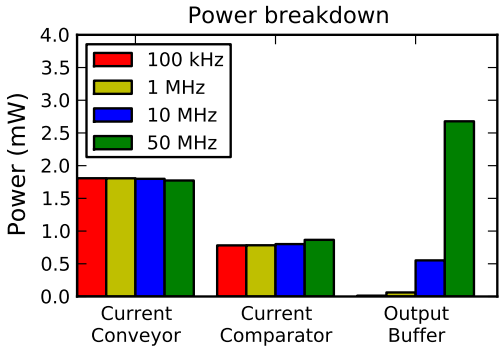

Figure 5. Power breakdown in the 3M2P 0.5 μm process.

and comparator transistors change as follows: $\frac{W}{L}_p = \frac{18\,\mu\text{m}}{0.6\,\mu\text{m}}$ to $\frac{18\,\mu\text{m}}{0.18\,\mu\text{m}}$ and $\frac{W}{L}_n = \frac{6\,\mu\text{m}}{0.6\,\mu\text{m}}$ to $\frac{4.005\,\mu\text{m}}{0.18\,\mu\text{m}}$. The transistors stay at about the same width but scale down in length. This is primarily due to both process circuits supplying the same I_{mtj} current for a constant R_{mtj}. The rail-to-rail output buffer transistors are scaled $^{0.5\,\mu\text{m}}/_{0.18\,\mu\text{m}} = 2.77$ times smaller which is the scaling factor between the two processes. The new layout has dimensions $8.28\,\mu$m by $27.27\,\mu$m. The area of the current conveyor and current mirror sub-circuits scale roughly linearly. The rail-to-rail output buffer may scale quadratically.

B. Transient Response

The transient response of the circuit limits the maximum frequency at which the read circuit can be clocked by an external magnetic field. For the R2V read circuit implemented in the 3M2P $0.5\,\mu$m process, the transient response is shown in Figure 4. The input resistance R_{mtj} is clocked at 10 MHz with values 500 and 1 kΩ. An appropriately chosen area and RA product of an MTJ device will yield these values. The bias voltage V_{bias} is set to 0.1 V which is pinned at V_{mtj}. The variation in V_{mtj} is due to non-linearities in the current conveyor circuit, which are not a concern for a global clocking application. I_{mtj} is measured to be 229.9 and 129.9 μA for each R_{mtj}. These states are distinguished by comparing I_{mtj} to a threshold current I_{th} indicated by the dashed line in the figure. Node $N1$ is not rail-to-rail since voltage is needed from drain-to-source of transistors M_{7-10} to keep them turned on.

Rise/fall times can be used to identify which node limits the maximum clock frequency of the global external magnetic field. The rise/fall times, measured from 10% to 90% between signal low and high, for $N1$, $N2$, and $MCLK$ are shown in Table II for implementations in both the 3M2P $0.5\,\mu$m and 5M1P $0.18\,\mu$m process technologies. Node $N1$ of the current comparator is shown to be the bottleneck node with a rise/fall time of 9.275/7.767 ns in the 3M2P $0.5\,\mu$m process. This is primarily due to the high impedance of the cascoded output stage of the current comparator that gives large RC time constants.

The propagation delay of the R2V read circuit measures the latency of reading the input resistance as sensed at the output. These are shown in Table II. $t_{p,rise2fall}$ is the propagation time from a rising transition of R_{mtj} to a falling transition of $MCLK$. Conversely, $t_{p,fall2rise}$ is the propagation time from a falling transition of R_{mtj} to a rising transition of $MCLK$.

The maximum clock frequency is limited by the high impedance and moderate capacitance at node $N1$. The peak-to-peak voltage of node $N1$ decreases as the frequency increases beyond about 30 MHz since the node can no longer fully charge and discharge. The 3 dB point is simulated to be about 67 MHz, which is an estimate of the maximum frequency at which the circuit can operate.

In the 5M1P $0.18\,\mu$m process, the rise/fall times and propagation delays are shorter with smaller transistor dimensions and node $N1$ having less capacitance. The 3 dB point is simulated to be about 105 MHz.

C. Power

The power consumed by the read circuit limits the number of read circuits that can be built in a given power budget. The circuit continuously sinks current and consumes power. The power consumed is 3.21/1.98 mW when R_{mtj} is low/high (500/1 kΩ). During switching, the instantaneous power spikes

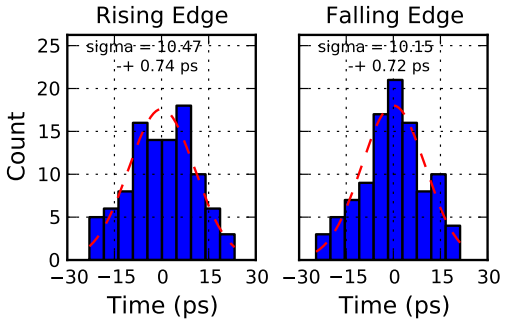

Figure 6. Jitter histogram of the rising/falling edges of MCLK due to noise in the 3M2P $0.5\,\mu$m process.

up due to dynamic power consumption in the output buffer. The average power consumed by this circuit at $10\,$MHz is $3.15\,$mW. A breakdown of the average power of each sub-circuit at varying clock frequencies is shown in Figure 5.

For the 5M1P $0.18\,\mu$m process, the current flowing through each branch of the current conveyor and current comparator remains the same, but the power supply is now operating at $1.8\,$V instead of $5\,$V. This results in less overall power consumed. At $10\,$MHz, the total average power is $0.647\,$mW.

D. Jitter

Noise from the transistors in the R2V read circuit contribute to jitter, an uncertainty in time, in the $MCLK$ output. Jitter on $MCLK$ contributes to the phase delay between two or more outputs. A Monte Carlo simulation is used to simulate the time-domain noise in the read circuit. Each noise source is replaced by a random variable and simulated in time. In the 3M2P $0.5\,\mu$m process technology, this simulation was done for 100 runs with thermal noise sources from $100\,$kHz to $1\,$GHz frequency. The jitter is calculated by measuring the delta time between when $MCLK$ output crosses $V_{DD}/2$ compared to the average crossing time. A histogram of the time jitter is shown in Figure 6 for rising and falling edges with an overlaid Gaussian normal PDF. The standard deviation, σ, of the jitter for the rising and falling edges is $10.47 \pm 0.74\,$ps and $10.15 \pm 0.72\,$ps, respectfully. For a Gaussian normal distribution, 99.7% of all random samples occur within $\pm 3\sigma$. Therefore, the jitter can be as high as $6\sigma \approx 62.8\,$ps for the rising edge or $6\sigma \approx 60.9\,$ps for the falling edge.

IV. Conclusion

We have designed an R2V read circuit to interface with MTJ devices. This circuit is characterized in terms of area, transient response, power, and jitter in the 3M2P $0.5\,\mu$m and 5M1P $0.18\,\mu$m process technologies. As the process scales down to smaller dimensions, area decreases, rise/fall times decrease, propagation times decrease, maximum frequency increases, power consumption decreases, and jitter decreases. A summary of these results is given in Table III.

From this investigation, we learned that the R2V read circuit has several areas for improvement. One, the $N1$ node of the current comparator has the highest rise/fall times, creating a performance bottleneck. A faster current comparator such as in [8] can be used to improve performance. Two, the power consumed and circuit area can be further reduced. Transistors M_{1-3} must provide I_{mtj} current flowing through it. But, transistors M_{4-10} could operate on less current, thus allowing these transistors to be made smaller.

A test chip was designed and fabricated. It is currently being tested for performance and to evaluate the feasibility of magnetic global clocking. The chip contains four read circuits and MTJs with phase delay between read circuits measured by an on-chip phase detector. The phase detector is designed using an array of symmetric XOR gates followed by buffers. The XOR gates produce the same pulse output on both rising and falling edges, independent of input arrival order. The buffer drives a pin capacitance of $8\,$pF with $1\,$ns rise/fall time. Simulation shows that delays above about $1.25\,$ns can be detected at the buffer output and are linear above $2\,$ns. The quality of phase measurements is affected by the symmetry of the XOR gates, delay through the buffers, variations in the MTJ devices and CMOS transistors, circuit noise/jitter, and wire delays. We suspect that the phase delay in the MTJ devices will be the most significant and plan to measure this on the test chip.

Table III
Summary of results. R=rise, F=fall

	3M2P 0.5 μm	**5M1P 0.18 μm**
Dim. of Layout	$31.35 \times 40.20\,\mu$m	$8.28 \times 27.27\,\mu$m
Area of Layout	$1,260.27\,\mu$m^2	$225.80\,\mu$m^2
f_{max}	$66.8\,$MHz	$105.0\,$MHz
$t_{N1,r/f}$ (10-90%)	$9.275/7.767\,$ns	$5.430/5.240\,$ns
$t_{N2,r/f}$ (10-90%)	$2.702/2.694\,$ns	$0.805/0.809\,$ns
$t_{MCLK,r/f}$ (10-90%)	$0.977/0.964\,$ns	$0.225/0.230\,$ns
$t_{p,r2f/f2r}$	$7.215/6.691\,$ns	$4.625/2.403\,$ns
$P_{avg,10\,\text{MHz}}$	$3.15\,$mW	$0.647\,$mW
$\sigma_{MCLK,jitter,r/f}$	$10.47 \pm 0.74\,$ps / $10.15 \pm 0.72\,$ps	$8.67 \pm 0.62\,$ps / $12.70 \pm 0.90\,$ps

References

[1] W. C. Black and B. Das, "Programmable logic using giant-magnetoresistance and spin-dependent tunneling devices (invited)," *Journal of Applied Physics*, vol. 87, no. 9, pp. 6674–6679, May 2000.

[2] M. Durlam *et al.*, "A 1-Mbit MRAM based on 1T1MTJ bit cell integrated with copper interconnects," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 5, pp. 769–773, May 2003.

[3] E. K. S. Au *et al.*, "A novel current-mode sensing scheme for magnetic tunnel junction MRAM," *IEEE Transactions on Magnetics*, vol. 40, no. 2, pp. 483–488, Mar. 2004.

[4] J. Slaughter, "Materials for magnetoresistive random access memory," *Annual Review of Materials Research*, vol. 39, no. 1, pp. 277–296, 2009.

[5] W. Zhao *et al.*, "High speed, high stability and low power sensing amplifier for MTJ/CMOS hybrid logic circuits," *IEEE Transactions on Magnetics*, vol. 45, no. 10, pp. 3784–3787, Oct. 2009.

[6] M. J. Hall, V. Gruev, and R. D. Chamberlain, "Noise analysis of a current-mode read circuit for sensing magnetic tunnel junction resistance," in *IEEE Int'l Symposium on Circuits and Systems*, May 2011.

[7] D. Freitas and K. Current, "CMOS current comparator circuit," *Electronics Letters*, vol. 19, no. 17, pp. 695–697, 1983.

[8] L. Chen, B. Shi, and C. Lu, "A robust high-speed and low-power CMOS current comparator circuit," in *IEEE Asia-Pacific Conf. on Circuits and Systems*, 2000, pp. 174–177.