Novel Numerical Representations for Low-Power Audio Signal Processing

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One of the major technical issues facing the designers of modern digital hearing aids is the need to minimize the power consumption of the system to prolong battery life. As new signal processing techniques are proposed, the computational requirements invariably grow, putting additional pressure on power consumption. In this work, we investigate the use of non-standard numerical representations for the audio signals being processed, showing how the power consumption can be lowered for audio signal processing while maintaining (and even improving) overall signal quality.

Standard numerical representations include fixed-point representations (typically 16 bits) and floating-point representations (either 32- or 64-bit IEEE standard). In this study, we compare the power consumption of a 16-bit linear representation with several different floating-point representations (4- to 6-bit exponent and 4- to 6-bit mantissa) and a 9-bit logarithmic notation. Each representation is tailored to provide a dynamic range of approximately 100 dB and a signal-to-quantization-noise ratio of approximately 30-35 dB (i.e., optimized for understanding of speech signals). The power consumption is investigated while computing a series of multiply-accumulate operations. The multiply-accumulate (MAC) is the most common computation in audio signal processing.

For each representation, we design a hardware MAC unit in the VHDL language and perform a standard-cell synthesis, layout, and place-and-route targeting the AMI Semiconductor 0.5 micron VLSI integrated circuit process. The resulting design is simulated using the Mentor Graphics MACH-PA power analysis tool, with input vectors modeling a 21-tap finite impulse response band-pass filter. The simulation output both verifies correct operation of the circuit and provides information on power consumption.

The results show a significant power savings (greater than 5x) using both the floating-point representations and the logarithmic representation. This is primarily due to the ability to either eliminate (in the case of the logarithmic representation) or significantly reduce the size of the hardware multiplier required as part of the MAC unit. We will present both novel techniques for implementing the accumulation function with a logarithmic representation as well as the power consumption associated with each numeric representation. [This work was supported by NIDCD].