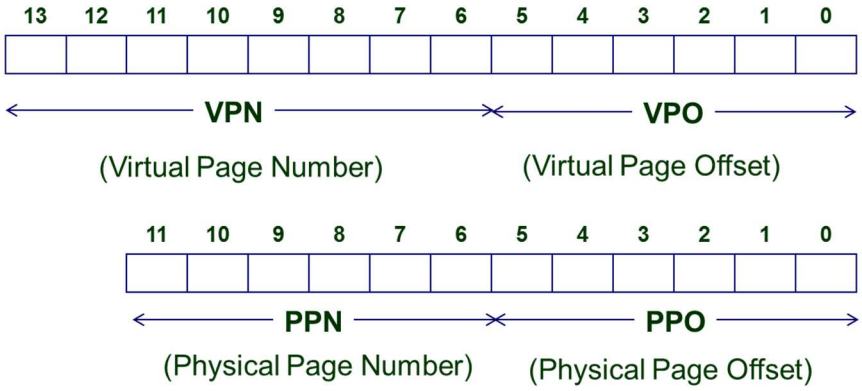
CSE 5600 – Practice Problem Set 8

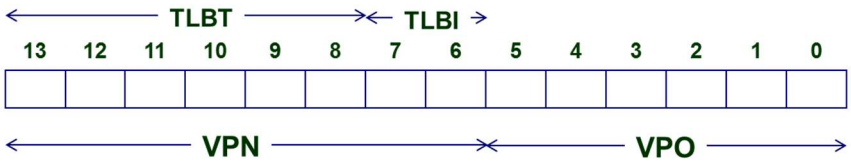
1. Consider the simple virtual memory system described below.
    - 14-bit virtual addresses
    - 12-bit physical addresses
    - Page size = 64 bytes



The first 16 entries in the virtual page table are shown below:

VPN	PPN	Valid	VPN	PPN	Valid
00	28	1	08	13	1
01	–	0	09	17	1
02	33	1	0A	09	1
03	02	1	0B	–	0
04	–	0	0C	–	0
05	16	1	0D	2D	1
06	–	0	0E	11	1
07	–	0	0F	0D	1

The TLB has 16 entries and is 4-way associative. We can understand access to the TLB by considering virtual addresses as follows:

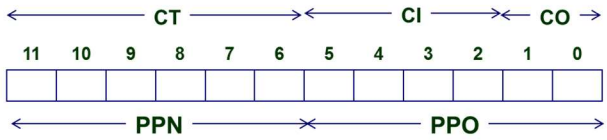


Here the TLBT is the tag bits and the TLBI is the index into the TLB.

The contents of the TLB are shown next.

Set	Tag	PPN	Valid	Tag	PPN	Valid	Tag	PPN	Valid	Tag	PPN	Valid
0	03	–	0	09	0D	1	00	–	0	07	02	1
1	03	2D	1	02	–	0	04	–	0	0A	–	0
2	02	–	0	08	–	0	06	–	0	03	–	0
3	07	–	0	03	0D	1	0A	34	1	02	–	0

The physically addressed cache is direct mapped. It has 16 lines (blocks) and a 4-byte line size.

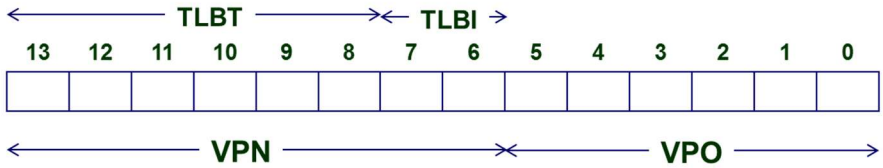


Here, CT is the cache tag, CI is the index, and CO is the offset.

The contents of the cache are:

Idx	Tag	Valid	B0	B1	B2	B3	Idx	Tag	Valid	B0	B1	B2	B3
0	19	1	99	11	23	11	8	24	1	3A	00	51	89
1	15	0	–	–	–	–	9	2D	0	–	–	–	–
2	1B	1	00	02	04	08	A	2D	1	93	15	DA	3B
3	36	0	–	–	–	–	B	0B	0	–	–	–	–
4	32	1	43	6D	8F	09	C	12	0	–	–	–	–
5	0D	1	36	72	F0	1D	D	16	1	04	96	34	15
6	31	0	–	–	–	–	E	13	1	83	77	1B	D3
7	16	1	11	C2	DF	03	F	14	0	–	–	–	–

(a) For virtual address 0x03D4, fill in the bits of the virtual address below (yes, in binary) and answer the associated questions.



What is the VPN (in hex)?

What is the VPO (in hex)?

What is the TLBI (in hex)?

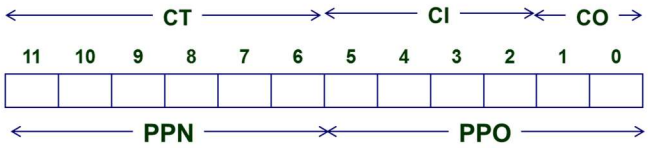
What is the TLBT (in hex)?

Does an access to this address result in a TLB hit?

Does an access to this address result in a page fault?

What is the PPN (in hex)?

If known, fill in the bits of the physical address below (yes, in binary) and answer the associated questions.



What is the cache offset (in hex)?

What is the cache index (in hex)?

What is the cache tag (in hex)?

Does an access to this address result in a cache hit?

If so, what is the byte value?

(b) Repeat part (a) for virtual address 0x0B8F.

(c) Repeat part (a) for virtual address 0x0040.

2. Starting from the standard equation for memory access time with a cache:

$$t_{avg} = t_{hit} + \%miss \times t_{miss}$$

Expand the equation to include the effects of virtual memory, including a TLB, and both an L1 and L2 cache. Be careful with the definitions of any variables you introduce.

You can assume that TLB access and L1 access happen concurrently.