Introduction to Digital Logic

- VHDL

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Review Problems

- Describe the difference between an entity and a component
- Describe the difference between an entity and an architecture
- Describe what a process is. How does VHDL behave differently with/without a process?
- What is a sensitivity list? What items should be included in it?

Review Problems

Draw a circuit that implements the following VHDL code segment, assuming *a-d* are all single bit signals

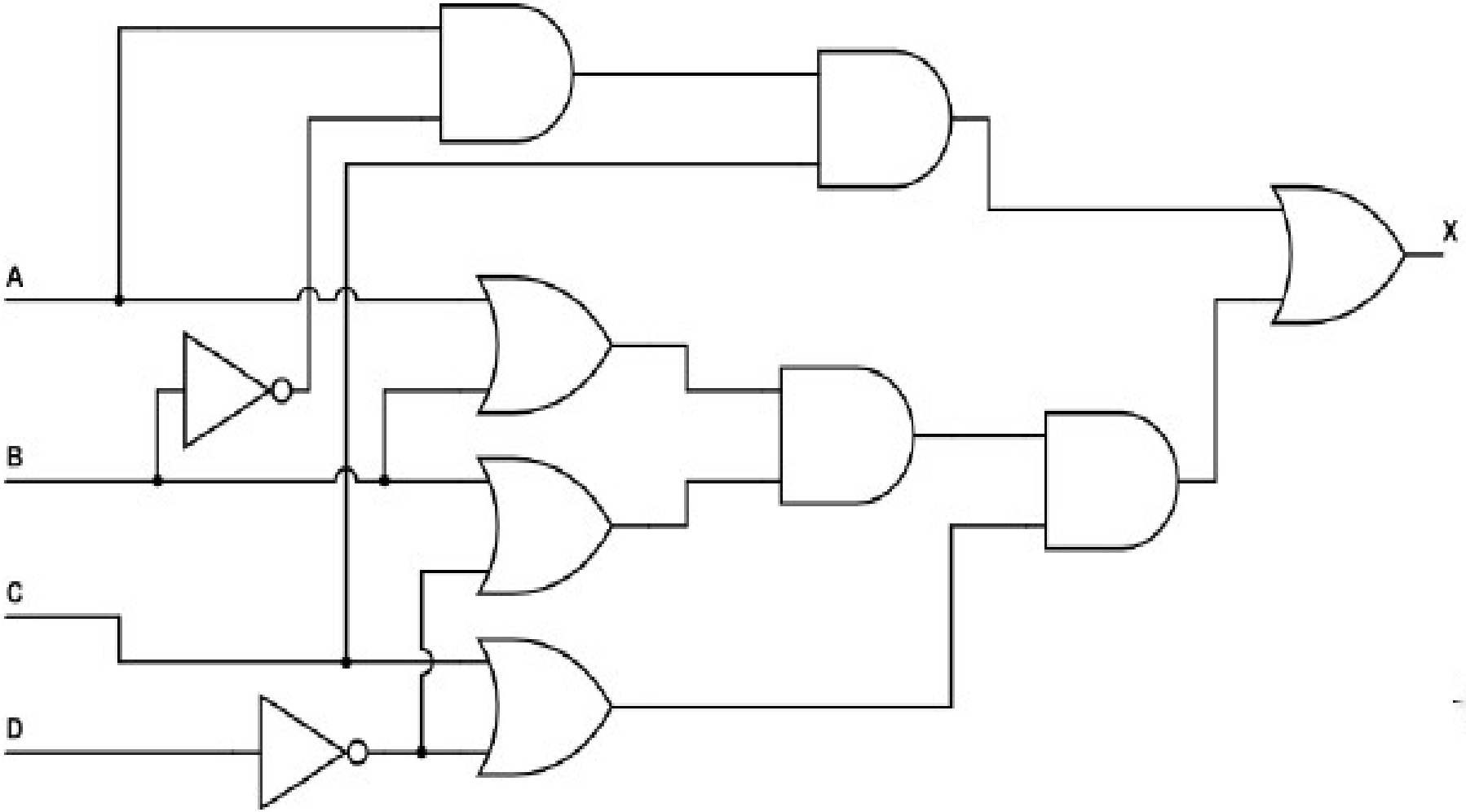
```
x <= a and b;
y <= x or (c and d);
z(0 to 1) <= (a and c) & (x or c);
```

Rewrite this code so that it combines *a-d* into a vector

Write VHDL code for each of the entities described above

Review Problems

- Write a VHDL code segment that is implemented by the circuit below:



Review Problems

Rewrite the following VHDL module using only ordinary signal assignments (no conditional assignments).

```
entity foo is port(
   a,b,c,d: in std_logic;
x: out std_logic;
y: out std_logic_vector
(1 downto 0);
end foo;

architecture arch of foo
begin
   x <= b and c when a='0' else
      not c when a>b else
      a or d;
   y <= (a & d) when a='1' else
      (b & (not c)) when (b='0' and c='1') else
      '1' & c;
end arch;
```

Review Problems

For the given truth table, create a circuit and implement it in VHDL. Use vectors where appropriate.

decimal	*BCD* *ABCD*	*xs3* *WXYZ*
0	0000	0011
1	0001	0100
2	0010	0101
3	0011	0110
4	0100	0111
5	0101	1000
6	0110	1001
7	0111	1010
8	1000	1011
9	1001	1100