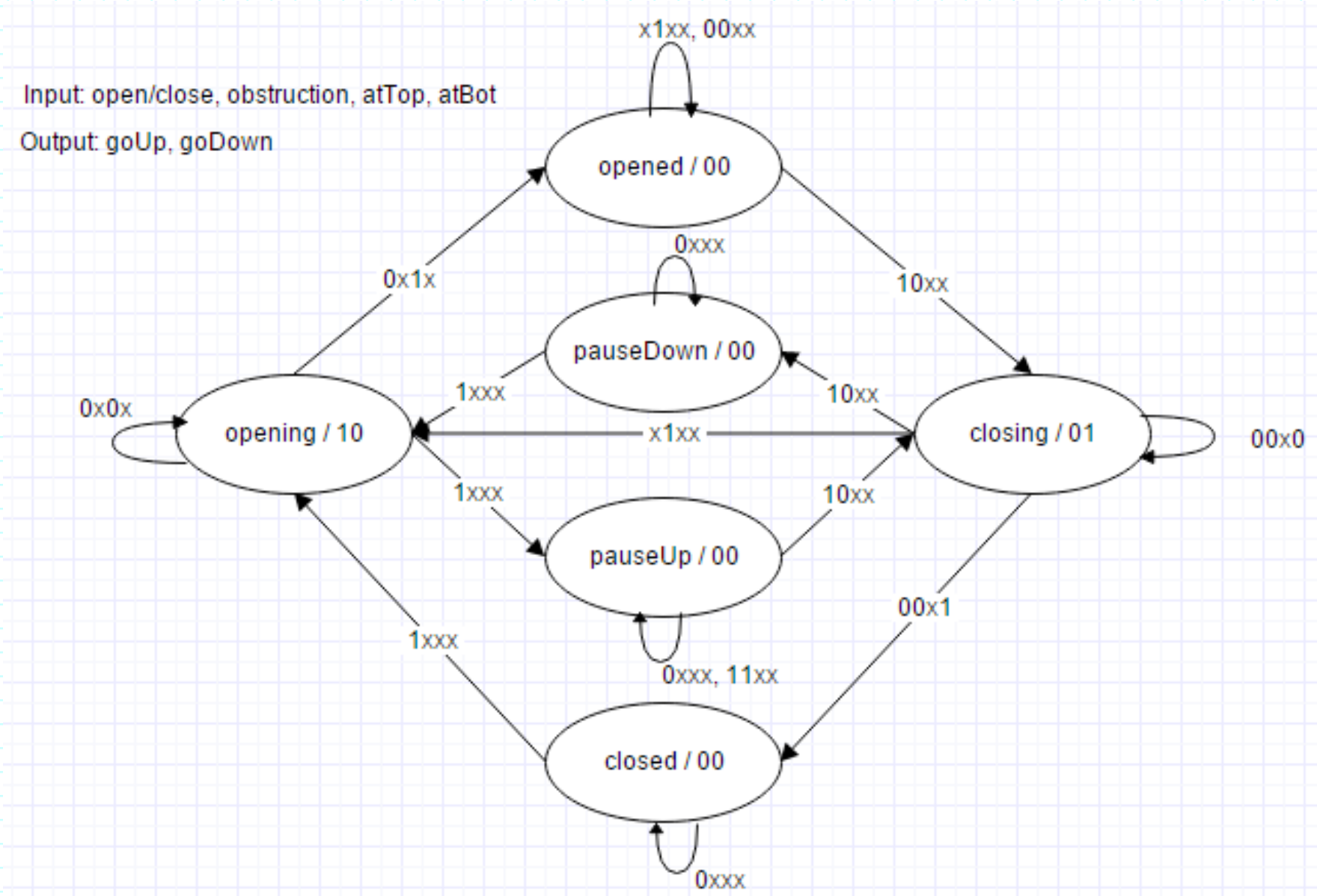
Introduction to Digital Logic

- FSM VHDL
- Timing

Doug Shook

Garage Door FSM Demo



Review Questions

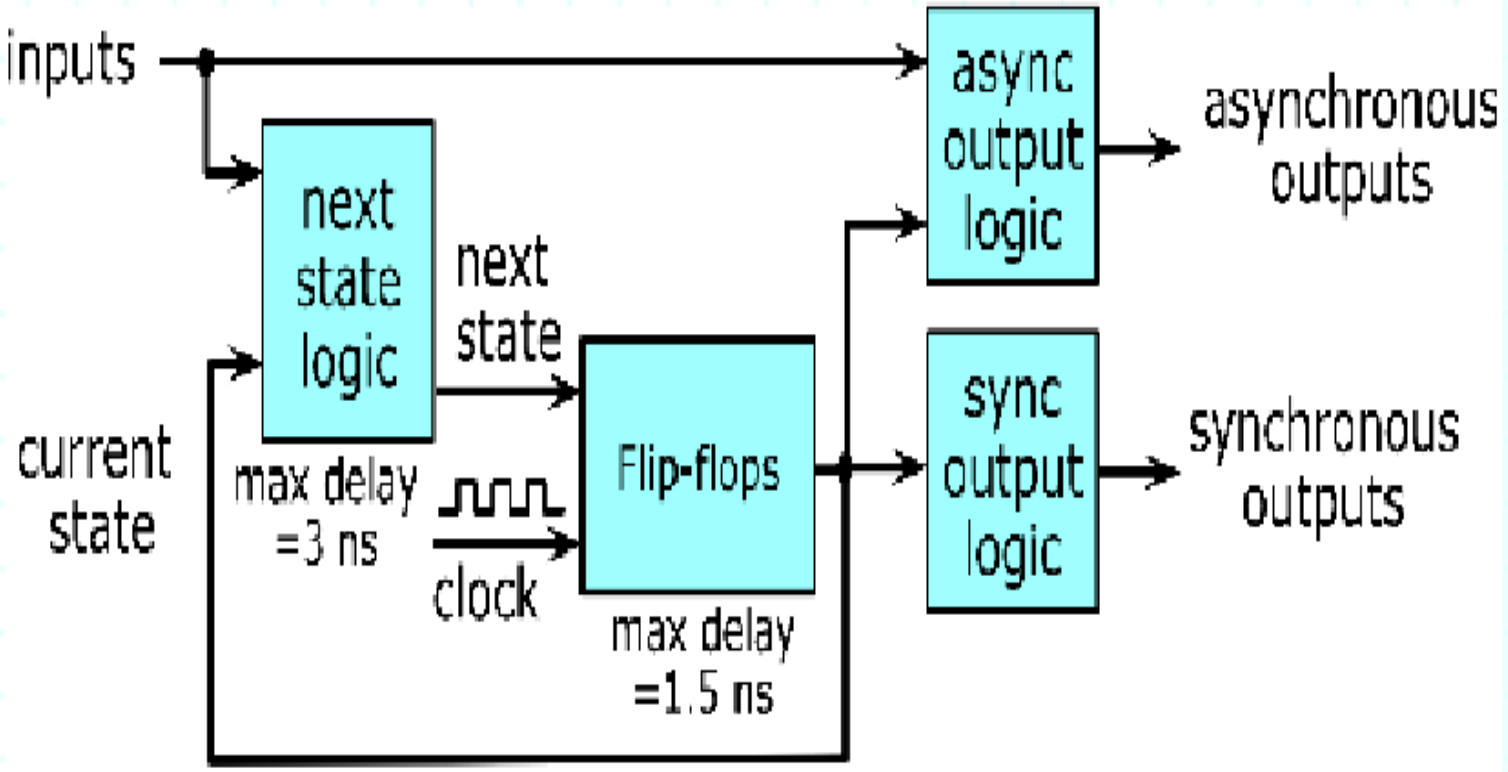
- What causes delay in digital circuits?
- What is setup time?
  - Why does it exist?
- What is hold time?
  - Why does it exist?
- Describe how to determine the clock speed of a circuit.

Review Questions

Consider a circuit in which there is a path from an input *x* to a flip flop that has a maximum possible delay of 7 ns, and there is also a path from *x* to another flip flop with a minimum delay of 3 ns. If the setup and hold times are 2 ns and 1 ns respectively and the clock input rises at time *t*, is it ok for *x* to change at time *t*–5? What about *t*–1? What about *t*? What about *t*–10?

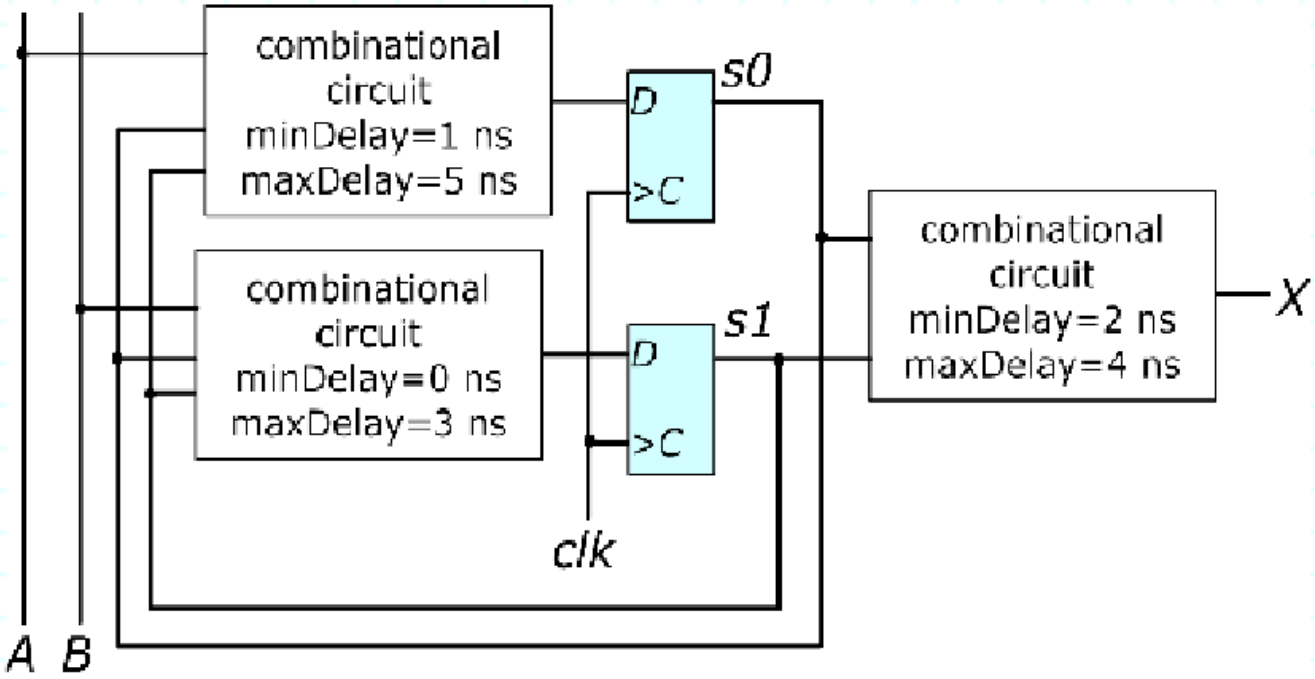
Review Questions

If the setup time for the flip flops is 1.5 ns and the maximum clock skew is .5 ns, what is the smallest clock period for which the circuit is guaranteed to work correctly?



Review Questions

For the state machine shown below, assume that the flip flop setup time is 2 ns, the hold time is 0.5 ns and the flip flop propagation delay is between 1 and 3 ns. Also, that the clock skew is 0.3 ns.



Is this circuit subject to internal hold time violations? What is the smallest clock period for which the circuit is not subject to setup time violations? If violations exist, determine how they could be fixed. What is the latest time relative to the clock, when it is safe for input *B* to change? What is the latest time after the clock when output *X* can be changing?

Review Questions

For the given circuit:

- Are there any hold time violations?
- What is the smallest possible clock period?
- If the clock goes from low to high at time *t:*
  - When must the inputs A and C remain stable?
  - When will the output Y change?

