Introduction to Digital Logic

- Exam II Review

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Topics

- Latches
  - SR, D
- Flip Flops
  - DFF, Registers
- FSM
  - Mealy, Moore, Minimization
- FSM Circuits
  - FSMs to Circuits, Circuits to FSMs

Topics

- State Encodings
  - Binary, One-hot
- Sequential VHDL
  - Process, case/when, LUTs
- Timing Issues
  - Setup, Hold Time, Clock Frequency, I/O
- Components
  - Adders, Subtractors, Comparators, Serial

Review Questions

- What is the difference between a synchronous circuit and a combinational circuit?
- How does an SR-Latch differ from a D-Latch?
- What is the difference between a D Latch and a D Flip-Flop?
- What is a register?
- What are the steps for developing an FSM?

Review Questions

- A computer can be thought of as having four states: off, running, power save, and sleep.
  - Construct an FSM:
    - What are possible inputs?
    - What are outputs?
    - What are the transitions?

Review Questions

- Can your FSM be minimized? If not, explain why.
- Write VHDL that implements your FSM.
- Draw a timing diagram for your FSM that shows each transition.

Review Questions

- Draw a circuit for your FSM that uses binary encoding.

- If we assume a propagation delay of 1-3ns, a gate delay of 1-4 ns, a hold time of 1ns, a setup time of 2ns, and no clock skew:
  - Are there hold time violations?
  - What should the clock period be?
  - When must the inputs be held stable?

Review Questions

- Construct a FSM that performs serial subtraction.
- Draw a circuit that implements this FSM using one-hot encoding.
- Analyze the timing constraints of your circuit using the timing information from the previous slide.
- Write VHDL code that implements your FSM.