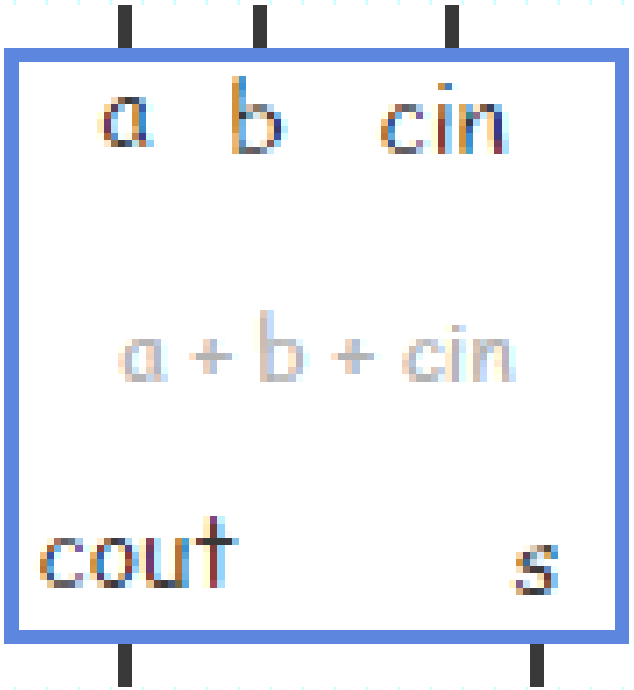
Introduction to Digital Logic

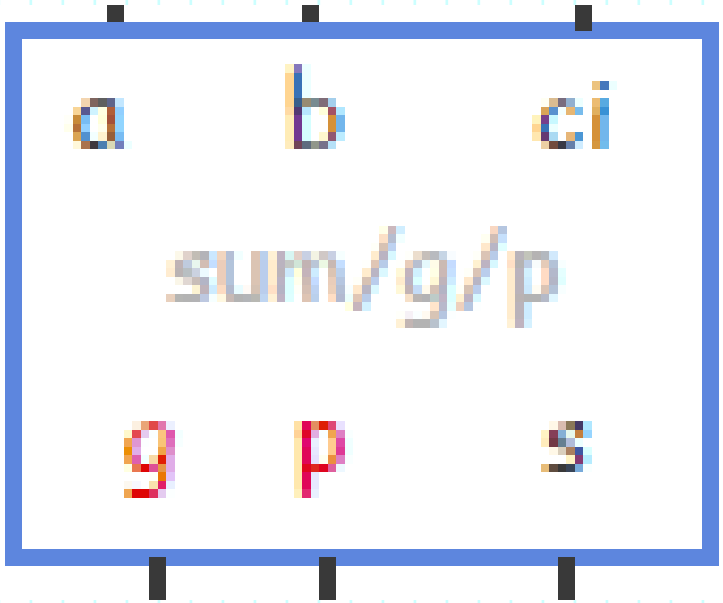
- Carry Lookahead Adders
- Multipliers

Doug Shook

Review Questions

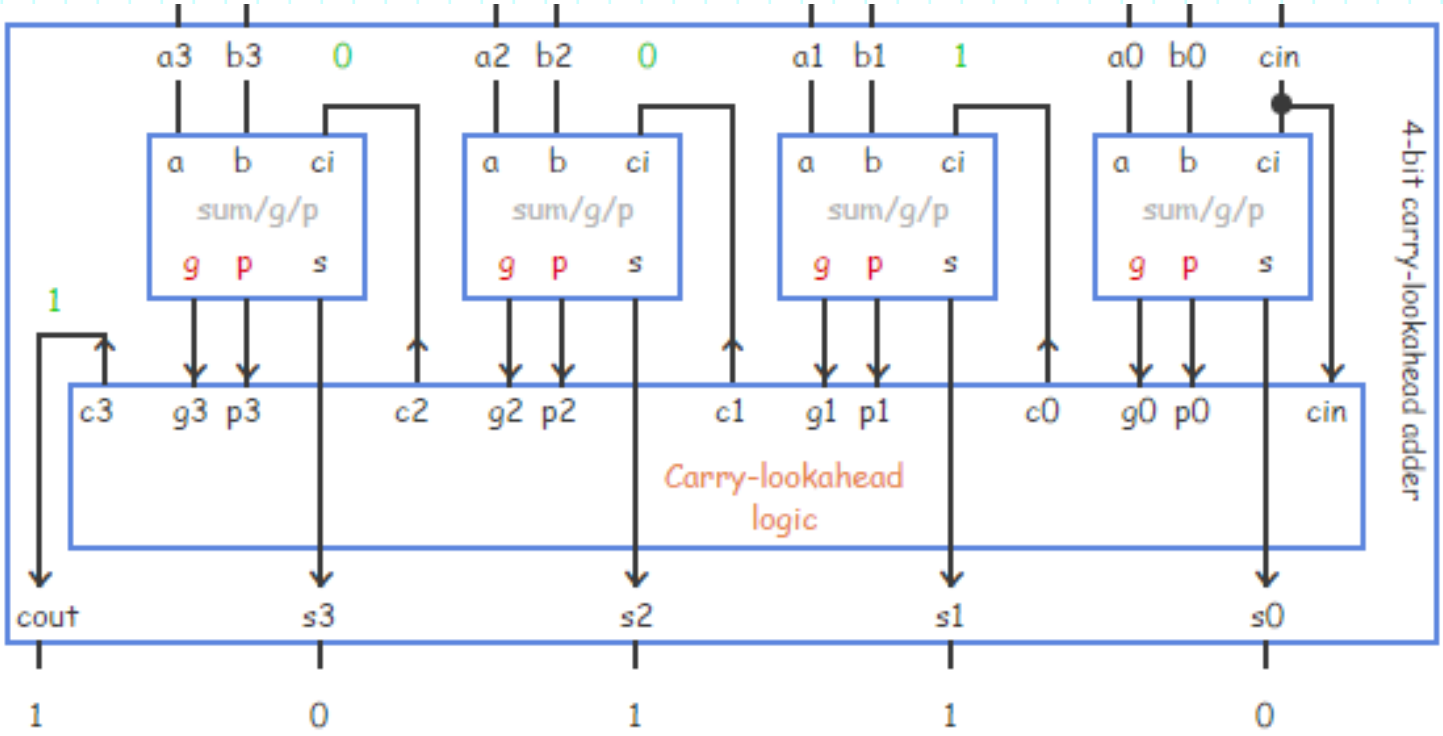
- How does the adder component compare in a carry ripple adder vs. a carry lookahead adder?





Review Questions

- Sketch a circuit for the lookahead logic



$c3 = g3 + p3c2$ $\quad c2 = g2 + p2c1$ $\quad c1 = g1 + p1c0$ $\quad c0 = a0b0 + (a0 + b0)cin$

$c0 = g0 + p0cin$

... ... $\quad c1 = g1 + p1(g0 + p0cin)$

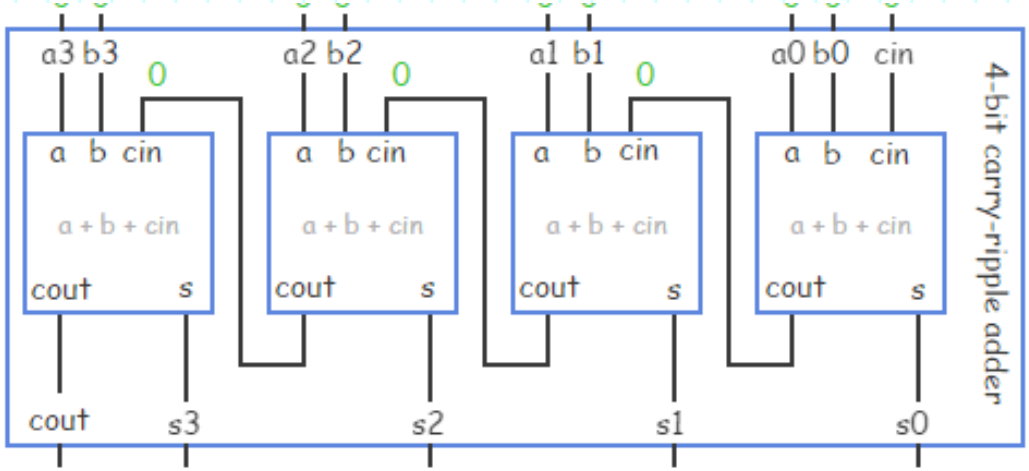
$c1 = g1 + p1g0 + p1p0cin$

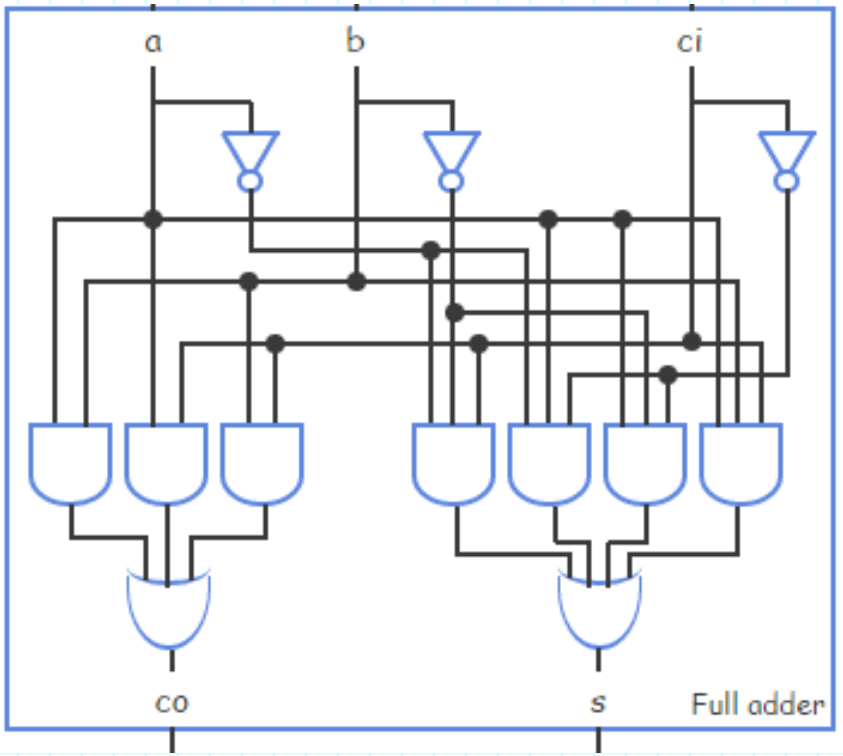
$c2 = g2 + p2g1 + p2p1g0 + p2p1p0cin$

$c3 = g3 + p3g2 + p3p2g1 + p3p2p1g0 + p3p2p1p0cin$

Review Questions

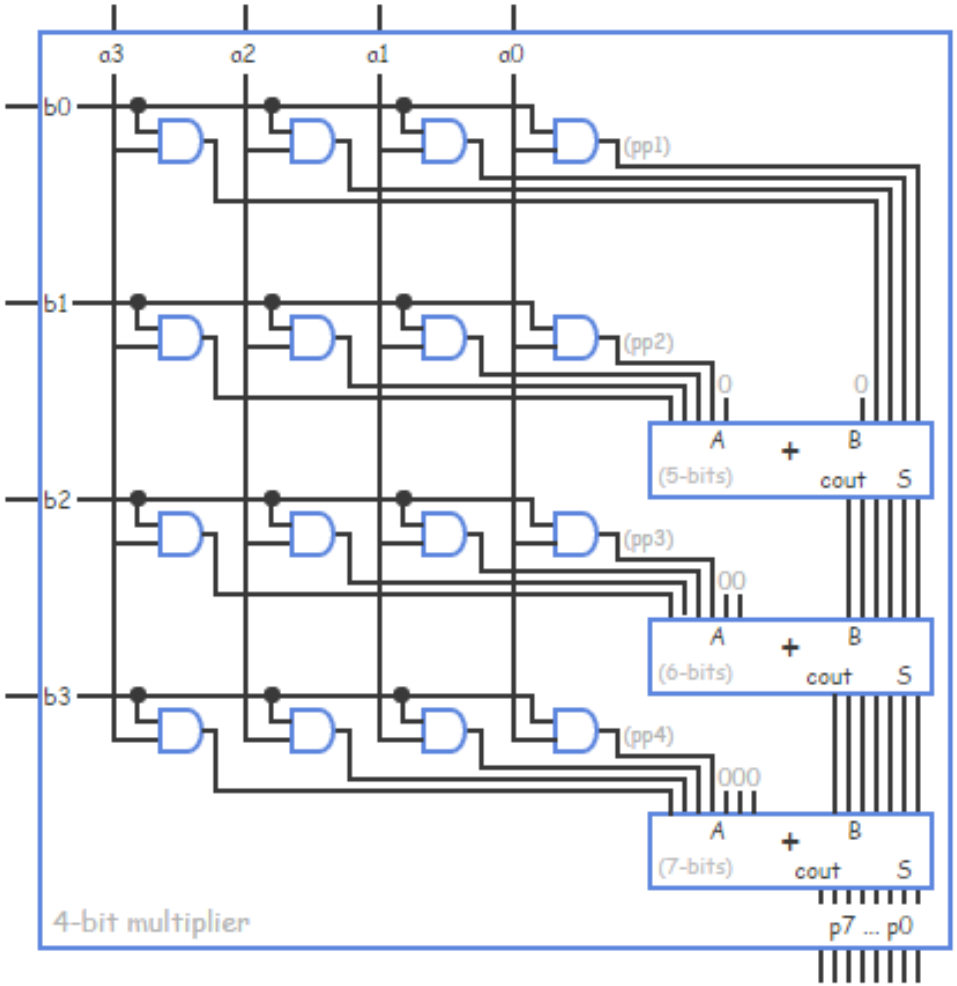
- Assuming a delay of 2ns per gate, how does the delay of a carry ripple adder compare to a carry lookahead? What is the worst case delay for each component? What is the best case delay for each component?





Review Questions

- What's the max delay of a multiplier circuit with carry ripple adders? What's the max delay with carry lookahead adders? Assume 2ns per gate.



Review Questions

- Consider a 4 bit signed binary value. If we wish to determine an equivalent signed binary value that uses 8 bits, what must we do? Design a circuit that implements this conversion.

Review Questions

- Can this multiplier handled signed binary values? If not, explain what modifications are necessary to handle signed binary.

