CSE260: Introduction to Digital Logic
Lab #4 Coversheet
Due: Tuesday, Nov. 17Th

Your Name _____

Your Partner's Name _____

Names of any students you discussed this lab with:

This section is to be filled out during the demo. TA Name_____

Component	Points (0-3) (3=perfect, 2= minor errors, 1=big problems, 0=not done)	Comments (if less than 3 points, the TA should explain why)
HLSM / Circuit	/ 3	
Stack VHDL	/ 3	
Test Bench	/ 3	
Simulation	/ 3	
FPGA Demo	/ 3	
Sub-Total	/ 15	**TA Signature: _____**

This section is to be filled out after the lab is turned in.

Hardcopy items: ☐ HLSM ☐ Circuit ☐ Simulation

Digital items: ☐ Stack Code ☐ Testbench ☐ top.vhd

TA Signature: _____