Pulse-modulated Radar Display Processor on a Chip

Talal K. Darwich and Charles D. Cavanaugh
Center for Advanced Computer Studies
University of Louisiana at Lafayette
{tkd7931, cdc}@cacs.Louisiana.edu

Abstract

As technology is going up day after day, equipments are getting compact more and more. So an idea of having radar on a chip becomes more important. A radar system is broken down into its circuit elements. This system shows how we can have a control on the minimum range detected by a software tool (LABVIEW) by simply moving a button instead of having a complicated circuitry for that. Also a display system implemented fully with the same software that can be transformed into FPGA is shown too as a step towards having radar system fully implemented on a chip. The use of software gives the flexibility in design as it can be applied to any radar without the need to change any parameter in the display system at all.

Introduction

There are several related works in which FPGA of [1] is used in sonar processing such as, time delay, frequency domain, and matched-field beam forming algorithms. Complex arithmetic is done in either rectangular or polar forms due to CORDIC algorithm mapping onto FPGAs. Parallel processing improvement is due to FPGAs multiple memory ports facilities and pipelining.

CORDIC (shift-add algorithm) is implemented using FPGA [2] to compute many functions such as trigonometric, hyperbolic, linear and logarithmic functions.

The proposed FPGA system of [3] is several times better than traditional system implemented by DSPs designed for multiprocessing systems due to the core easy calculation, the DSP’s address hardware calculation shortage and the simple customizing of FPGA I/O to the application.

In [4], an FPGA is used to compute the intensive middle stage—the complex phase shifts and accumulations— that can be used with data in either rectangular or polar format.

A sonar spectrum recognition chip is implemented using FPGA by transforming sonar spectrum into truth tables. Achieved speed of the chip was less than 1.0 microsecond per spectrum. The chip achieved the recognition accuracy of 91.7%, which was higher than those in the back-propagation and the K-NN algorithm [5].

As we can see that FPGA has been used to have higher speed. So in this paper we proposed a design for the display of sonar or any radar system implemented by LABVIEW that can be transformed into FPGA. Also it is a step towards having radar on a chip.

The word radar stands for Radio Detection And Ranging. It is used to detect moving and stationary objects in many civil and military applications such as aircrafts, ships and ground stations.
Radars consist of three subsystems transmitter, receiver and a display subsystem. The transmitter circuit radiates radio waves in the space through the antenna. The signal will move in the space and will be reflected back by the presence of an object. The receiver antenna will receive the reflected signal and signal-processing techniques will be applied to calculate the range, speed and height of the detected target. Then this information is sent to the display circuitry to be visualized on screens.

**Pulsed radar**

The Pulsed radar sends pulses of radio waves for a small period of time $T_0$ then stops sending signal for a longer interval of time $T_1$ as shown in figure 1. The whole period is $T = T_0 + T_1$. The transmitter will be working while sending the signal and the receiver gator shuts down the receiver. The pulsed radar is broken down into its circuit elements in the following sections.

![Figure 1. Radar Pulse Modulated Signal.](image)

**Transmitter**

The transmitter consists of a timing pulses circuit, an oscillator, transmitter gator and transmitting antenna as shown in figure 2.

Timing circuit: It is composed of a 555-timer chip. The frequency is 14Hz and the period is 71ms. The pulse width is 3.5ms and the duty cycle is 4.93 %.

Oscillator: It is a Wein bridge oscillator that uses a positive feedback loop of an ap-amp. The carrier frequency is 40 KHz.

![Figure 2. Transmitter.](image)
Transmitter Gator: It is composed of three NPN transistors as shown in figure 3. The oscillator output is connected to the collector of Transistor T1 (Vin) through a capacitance. The output (Vout) is taken from the emitter of the same transistor T1 and it is connected to the transmitter. The output of the timing circuit is connected to the base through a resistance to have the pulsed signal controlling the gator circuit. To have sharper edge at the fall down in the output signal, a transistor is used to sink more current. So this transistor T2 should be on or sinking current when the timing circuit pulse is low and off when the timing circuit pulse is high. This transistor T2 must be controlled by a signal complement to the gator-controlling signal. And this leads to the use of transistor T3 to have the complement signal.

Receiver

The receiver consists of a receiving antenna, two amplifiers, gator 2, detector and two comparators as shown in figure 4.
Amplifier 1: The echo is fed to amplifier 1 which is a common emitter of gain 200. Receiver Gator: The output of amplifier 1 is fed to the collector of the transistor through a capacitance as shown in figure 5 and the output of the timing circuit is fed to the base. The emitter is connected to the ground. And the output is taken from the collector. This circuit will insure that the signal from the transmitter that is received when the transmitter was on is shorted to the ground.

![Receiver Gator Circuit](image)

Figure 5. Receiver Gator Circuit.

Amplifier 2: The output of the receiver gator circuit is fed to this amplifier, which is a common emitter of gain 200.

Comparator 1: It uses an op-amp with one of its input is connected to the output of amplifier 2 and the other input is connected to a threshold to get rid of the noise generated by the amplifiers and to have only one sided signal (the positive part only).

Detector: It is a rectifier circuit composed of a diode and a capacitance as shown in figure 6. It is used to get the envelope of the wave the low frequency component and get rid of the carrier frequency.

![Detector](image)

Figure 6. Detector.

Comparator 2: It uses an op-amp with one of its input is connected to the output of the detector and the other input is connected to ground to have clean pulses which will be the digital input to the DAQ board.

Display

The display consists of a DAQ board, software program and an indicator shown in figure 7.
Figure 7. Display.

DAQ board: It is used as an interface with the computer to read the echo signal and the gator.

Figure 8. Front Panel.

Software: LAB View is used to implement the display system and it consists of a software part
integrated with a hardware part as shown in figure 8 and 9.

The Front Panel is shown in figure 8. This interface contains buttons to control the angle the radar uses: pulse duration and the period, azimuth and vertical step increment, minimum range to be detected, (SONAR / EMW) switch. The indicators are: number of targets, distance and time for the target, ground range and height of the target, and elevation angle. There are also three charts one for the radial target, the plan position indicator (ppi) and the vertical plan indicator.

Figure 9. Block Diagram.

In this implementation, the transmitter Gator signal is used to trigger the reading of the echo signal. After detecting a one on the gator signal, the code starts monitoring the echo signal to calculate time and distance, where the starting point of measurement can be controlled or set by the user. In this scheme, this prototype can detect multiple targets where each target is represented by the detection of a zero-to-one transition or rise in the echo signal. The time is measured and consequently the range is calculated. The multiple targets are displayed using an indicator, which is designed using the same software.
Indicator: The display software is flexible; it can control the time of display and other factors. One of the controllable factors is the target elimination that can be used to eliminate the first \( n \) targets in a certain direction. In other words, it can replace the gator at the receiver side. Since the role of the gator is to eliminate the signal of the transmitter when it is on. So we can set up the minimum range to be detected. And having the gator implemented in software is much better than having it implemented by using hardware components. That will save power consumption, enhance the speed of the system, lower the design complexity, eliminate the noise generated by these components, increase the system controllability and simplify it. As a change in the gator pulse is needed, it is easy and achievable by just pressing the required button provided by the software interface, while it is hard in the hardware since it needs large value of components to insure wide range and will not give exact results as given by the software.

Breaking the block diagram shown in figure 9 down into its sub circuits to see the flow of design, the code consists of two `while` loops and one `for` loop embedded in a `while` loop to have continuous run until the stop button is hit in the front panel.

The first `while` loop shown in figure 10 monitors the gator signal when a high signal is read, the execution is terminated and a signal is sent to the second `while` loop to start running.

![Figure 10. Gator Detecting Circuit.](image)

The second `while` loop consists of circuits shown in figure 11, 12 and 13. Echo signal is monitored as shown in figure 11. The logic used below is to detect a rise from zero to one, which means a target is detected. Also the starting point is being taken care of by the same logic circuit.

![Figure 11. Echo Detecting Circuit.](image)
The signal at certain iteration is detected and compared with the previous iteration signal that has been stored in a buffer. If the comparison gives one and satisfies the condition of the starting point a one is fed to the adder that counts the number of targets between to gator signals.

Figure 12 is used to calculate the time and consequently the range of a target is measured. The if statement that calculate time and measure the range is controlled by the input parameter \( x \). When a target is detected, \( x \) is set to one allowing this statement to execute. The duty cycle is calculated in this part of code.

![Image of code](image)

Figure 12. Time and Range Measuring Circuit.

The circuit shown in figure 13 is used to control the while loop to terminate it when a high gator signal is monitored. When the gator signal is high, the first while loop terminates and the second while loop starts execution. At the end of the first iteration of the second while loop this circuit is executed. A high signal is detected as the gator pulse has a duration \( T_0 \) (figure 1) forcing the while loop to be terminated ending with a dead lock and the code will not run at all. To overcome this problem, the calculated duty cycle is evaluated in terms of number of iterations and compared with each iteration number. The detected gator signal is granted the control of the while statement when the iteration number is greater than the duty cycle corresponding iteration number.

![Image of circuit](image)

Figure 13. Gator Detecting Circuit and Duty Cycle Bypass Circuit.

The second while loop outputs the number of targets and corresponding ranges to the for loop takes the targets and tracing them in the indicator as shown in figure 14. It calculates the azimuth and the elevation angles and consequently the target height and ground range based on the step increment used by the radar antenna specified by the user through the front panel.
Figure 14. Tracing Circuit.

Figure 15 shows a statement that chooses between SONAR and EMW radar in terms of their speed and ranges.

```c
float r, s;
if(c==1)
  s=341;
else
  {s = 300000;
   sti = sti * 1000;
  }
r = s*p/2000;
a = r/n;
sto = sti * n*r;
```

Figure 15. SONAR and EMW Radar Statement.
Conclusion

This design will fit more in the design of radar on a chip, as a future work to have radar built on a chip. The labview software is used which can be transformed into FPGA and then downloaded on a chip. The whole display circuits can be designed on a chip and thus the external display circuitry is avoided.

References


Talal K. Darwich received the M.S. in computer engineering from the University of Louisiana at Lafayette and the B.S. in Telecommunication and electronic engineering from the Beirut Arab University in 2002 and 1998, respectively. He is currently a Ph.D. candidate with the Center for Advanced Computer Studies (CACS) at the University of Louisiana at Lafayette. He has been a Research Assistant with the CACS, in the VLSI Research group of M. Bayoumi from 2000 to 2002 and in the Radar Research group of C. Cavanaugh since 2003.

Charles D. Cavanaugh received the Ph.D. degree in Computer Science from the University of Texas at Arlington in 2000, the M.S. and B.S. degrees in Computer Science from the University of Texas at Tyler in 1997 and 1995, respectively, and the A.A. degree in Interdisciplinary Studies from Tyler Junior College in 1993. Currently, Dr. Cavanaugh does research in the areas of distributed real-time systems and embedded systems targeting mission-critical applications. He has been Assistant Professor in the Center for Advanced Computer Studies since Fall 2002. Dr. Cavanaugh is a member of the IEEE Computer Society and the ACM. Dr. Cavanaugh is also a member of Tau Beta Pi Engineering Honor Society, Alpha Chi National College Honor Society, and Kappa Delta Pi International Honor Society in Education.