entity reg_4 is
  port (d0, d1, d2, d3, clk, en: in bit;
       q0, q1, q2, q3: out bit);
end reg_4;

architecture struct of reg_4 is
  signal int_clk: bit;
begin
  and2_behavior: process is
  begin
    int_clk <= en and clk after 2 ns;
    wait on en, clk;
  end process and2_behavior;

  bit0:entity work.d_latch(basic)
    port map(d0, int_clk,q0);
  bit1:entity work.d_latch(basic)
    port map(d1, int_clk,q1);
  bit2:entity work.d_latch(basic)
    port map(d2, int_clk,q2);
  bit3:entity work.d_latch(basic)
    port map(d3, int_clk,q3);
end architecture struct;