CSE 568: Imaging Sensor
Final Project

1. CMOS voltage mode imaging sensors

The objective of this project is to design a complete imaging sensor. The imaging sensor can operate in voltage or current mode. The project will incorporate design of the pixel and read-out circuitry. The read-out circuitry will be composed of digital scanning registers, amplifiers, biasing circuits, etc. The imaging array will be composed of 100 by 100 pixels and the read-out speed should be 100 frames per second. The sensor will be designed in AMI 0.6 micron technology.

The project has to address the following criteria:

(a) Design a pixel that produces a linear output with respect to incident photons. The peripheral support circuitry should allow the pixel to operate in the linear mode.
(b) You will evaluate tradeoffs in your design between: pixel linearity, dynamic range of the output and power consumption of your imager.
(c) You will evaluate the three above mentioned tradeoffs when using: a) single current mirror and b) cascade current mirror for biasing the source follower in the pixel.
(d) Design the read out circuitry such that the imager is clocked at 1MHz. This read out frequency will allow frame rate of 100fps on 100 by 100 pixels.
(e) Design all digital circuitry necessary to operate the imaging sensor.
(f) Simulate all digital and analog circuits of your design.

You will have to complete three milestones and turn in progress reports for these milestones. These progress reports will be counted toward your final grade of the project. You will form groups of two students per team and will turn in one report per group for each milestone.

Milestones for all projects

**Part 1: due Thursday April 3rd, 2014.** Draw the three transistor pixel as presented in class in Cadence. Print the schematic of the pixel. Perform a transient simulation of the pixel. The integration time for the pixel should not exceed 10 msec. Perform transient simulations for photo currents: 10fA, 100fA and 1pA. You will need to reset the pixel and integrate photo charges on the photodiode. Plot the output of the source follower as a function of integration time. Import the output of the pixel in MAthlab and compute the non-linearity. Comment on the linearity of the pixel’s output and how it can be improved.

**Part 2: due Thursday April 10th, 2014.** Design a d flip flop circuit in Cadence schematic. Draw a symbol for the flip flop. Note: the online Cadence tutorial will guide you how to create a symbol for a given schematic. Present transient Spice simulation of the d flip flop operation. Print both the schematic and symbol of the d flip flop. Plot the transient results of the flip flop.

**Part 3: due Thursday April 17th, 2014.** Design a shift register composed of 100 d flip flops and an array of 100 by 100 pixels. Print the schematic for both designs. Perform a transient simulation on the shift register. All flip flops should start from value 0 and a single 1 will be loaded in the shift register. Clock the shift register 10 times. Present the simulation results.

**Part 4: due Thursday April 24th, 2014.** Put together the imaging array with the shift registers and read-out circuitry. Simulate the read-out of the first 3 pixels in the first row of the imager. Set the photo currents of the three pixels to be different. Hence, the output value from each pixel should be different and the simulation results should indicate this. Label clearly on your plots the output values of each pixel.
Final Report: due Monday 5:00pm, May 5th, 2014. Turn in a final report of your project. The report should connect the results from all four milestones into a single coherent report. Describe the objective of the design, the challenges, simulation results and concluding remarks. You will email me the final report.