Digital Integrated Circuit Design and Architecture

Chapter 1: Introduction
Some History

• Invention of the transistor (BJT) 1947
  – Shockley, Bardeen, Brattain – Bell Labs

• Single-transistor integrated circuit 1958
  – Jack Kilby – Texas Instruments

• Invention of CMOS logic gates 1963
  – Wanlass & Sah – Fairchild Semiconductor

• First microprocessor (Intel 4004) 1970
  – 2,300 MOS transistors, 740 kHz clock frequency

• Very Large Scale Integration 1978
  – Chips with more than ~20,000 devices
More Recently

Ultra Large Scale Integration

System on Chip (SoC)

20 ~ 30 million transistors in 2002

The chip complexity has increased by a factor of 1000 since its first introduction, but the term **VLSI** remained virtually universal to denote digital integrated systems with high complexity.
As a result of the continuously increasing integration density and decreasing unit costs, the semiconductor industry has been one of the fastest growing sectors in the worldwide economy.
Industry Trends

More portable, wearable, and more powerful devices for ubiquitous and pervasive computing…

High performance
Low power dissipation
Wireless capability
etc…
Some Leading-Edge Examples

First microprocessor (Intel 4004) 1970
2,300 MOS transistors, 740 kHz clock frequency

Intel Pentium 4
0.13μ process
55 million transistors
2.4GHz clock
145mm²
Cross section of 5 Layer IC
Evolution of Minimum Feature Size

Complexity - #transistors double every two years. 400M transistors and 64 Gbit memories in 2004.

Operating speed - double every two years. 5Gbits/sec 2002/03 and 10Gbits/sec 2003/04.

Design - each transistor hand crafted to design automation and reuse of cells.
“As long as downward scaling of CMOS technology remains strong, other technologies are likely to remain the technology of tomorrow.” - Intel Research Scientist

from http://www.intel.com/technology/mooreslaw/?iid=search
Future Technologies:

- 3-D Integration of 3 ICs
- Challenges:
  - How to design 3-D chips?
  - CAD Tools
  - Testing
  - Yield and Power Dissipation
Nano technology

Semi conductor nanowires fabricated using soft lithography
WashU CSE 2009

Chemical synthesis of semiconductor nanowires
WashU Chem. 2007

Challenges: Can we design circuits using semiconductors nanowires?
Metamaterials: Nano-Circuits

Pros: Operating frequency at Peta hertz
Challenges: reliable and repeatable fabrication
Integrated Detection Platform

- Digital Processing
- A/D Conversion
- Analog Processing
- Readout
- Sensing
- Optical Filtering
- Imaging Optics
- Object + Light Source

Integrated micro-channels and wells for reagent delivery and confinement
Integrated detection and analysis CMOS image sensor chip
Integrated Digital ICs with Nanotech for Medical Apps

Designing High-Performance Neural Prostheses
Neural Prosthetic Systems Laboratory (Shenoy Group), Stanford University

Problem: Millions of people are unable to move due to neurological injury and disease.
Solution: Bypass injury by using neural signals (from the brain) to control prosthetic devices.
Life Cycle of ICs

- Design
- Production

Circuit Performance vs. Time

Technology Window 1

Technology Window 2

longer design time for better performance in current generation

missed technology window = lower performance in next generation
VLSI Design Styles

Full-custom

Semi-custom
  - Cell-based (CBIC) (standard cells)
  - Masked gate array (MGA)

Programmable
  - PLD
  - CPLD
  - FPGA
Design Cycle: The Y - Chart
Imager RD planning

1 Mega Pixel Camera
- area: 1/4"
- power <100mW
- read out speed: 100fps
- SNR: 42dB

<table>
<thead>
<tr>
<th>Technology</th>
<th>TSMC 100nm</th>
<th>TSMC 180nm</th>
<th>IBM 350nm</th>
<th>AMS 1500nm</th>
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<tr>
<td>$/mm²</td>
<td>40K</td>
<td>5K</td>
<td>1.2K</td>
<td>1K</td>
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<tr>
<td>Basic block</td>
<td>1.8micron pixel</td>
<td>2.5micron pixel</td>
<td>3.5micron pixel</td>
<td>15micron pixel</td>
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<tr>
<td>Total IC area</td>
<td>1.8mm x 1.8mm</td>
<td>2.5mm x 2.5mm</td>
<td>3.5mm x 3.5mm</td>
<td>15mm x 15mm</td>
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<tr>
<td>$</td>
<td>130k</td>
<td>62k</td>
<td>15k</td>
<td>225k</td>
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<tr>
<td>Operation Speed</td>
<td>2GHz</td>
<td>1GHz</td>
<td>0.7GHz</td>
<td>0.4GHz</td>
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Simplified VLSI Design Flow

1. System Requirements
2. Architecture Definition and Logic Design
3. Design Verification
   - FAIL
   - Logic Diagram/Description
5. VLSI Design and Layout
   - FAIL
   - Verilog
6. Design Verification
   - PASS
   - Technology Design Rules Device Models
7. Mask Generation
8. Silicon Processing
9. Wafer Testing, Packaging, Reliability Qualification
Structured Design Principles

• **Hierarchy:** “Divide and conquer” technique involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.

• **Regularity:** The hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible. Regularity usually reduces the number of different modules that need to be designed and verified, at all levels of abstraction.

• **Modularity:** The various functional blocks which make up the larger system must have well-defined functions and interfaces.

• **Locality:** Internal details remain at the local level. The concept of locality also ensures that connections are mostly between neighboring modules, avoiding long-distance connections as much as possible.