

CSE/ESE 569M
Parallel Architectures and Algorithms
Assignment #5

Due: April 23, 2009.

1. Consider a four-processor bus-based multiprocessor using the Illinois MESI protocol. Each processor executes a test&set lock to gain access to a null critical section. Assume the test&set instruction always goes on the bus and it takes the same time as a normal read transaction. The initial condition is such that processor 1 has the lock and processors 2, 3, and 4 are spinning on the caches waiting for the lock to be released. Every processor gets the lock once and then exits the program. Considering only the bus transactions related to lock-unlock operations:
 - (a) What is the least number of transactions executed to get from the initial to the final state?
 - (b) What is the worst-case number of transactions?

You may assume the following: in the Illinois protocol, test&set invalidates other cached copies when it succeeds but only generates a read when it fails.

2. Suppose all 16 processors in a bus-based machine try to acquire a test-and-test&set lock simultaneously (and only once each). Assume all processors are spinning on the lock in their caches and are invalidated by a release at time 0.

How many bus transactions will it take until all processors have acquired the lock if all the critical sections are empty (i.e., each processor simply does a LOCK and UNLOCK with nothing in between)?

3. Give an example reference stream showing cache inclusion violation for the following situations:
 - (a) L1 cache is 32 bytes, two-way set associative, 8-byte cache blocks, and LRU replacement. L2 cache is 128 bytes, four-way set associative, 8-byte cache blocks, and LRU replacement.
 - (b) L1 cache is 32 bytes, two-way set associative, 8-byte cache blocks, and LRU replacement. L2 cache is 128 bytes, two-way set associative, 16-byte cache blocks, and LRU replacement.
4. Suppose a 16-way SMP lists at \$10,000 plus \$2,000 per node, where each node contains a fast processor and 128 MB of memory. How much does the cost increase when doubling the capacity of the system from 4 to 8 processors? From 8 to 16 processors? If an application has a parallel efficiency of 0.5 at 8 processors and 0.3 with 16 processors, is it more cost effective to purchase an 8 processor system or a 16 processor system?