

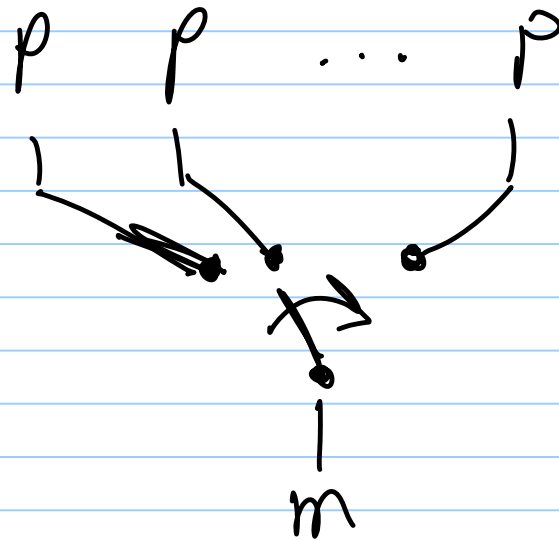
# Memory Consistency (cont.)

Note Title

4/9/2009

Seq. consistency

- maintain program order for each process
- $\exists$  sequential order among all operations



## Relaxed Consistency Models

2 approaches: "issue" vs. "view"  
to understand

### Issue

- e.g., - allow read or write to issue before prev. write is complete
- allow read or write to issue before prev. read is complete

DASH allows read to issue early, prior to:  
prev. write  
write propagating everywhere

called "processor consistency"

focus on  
allowed order of  
ops

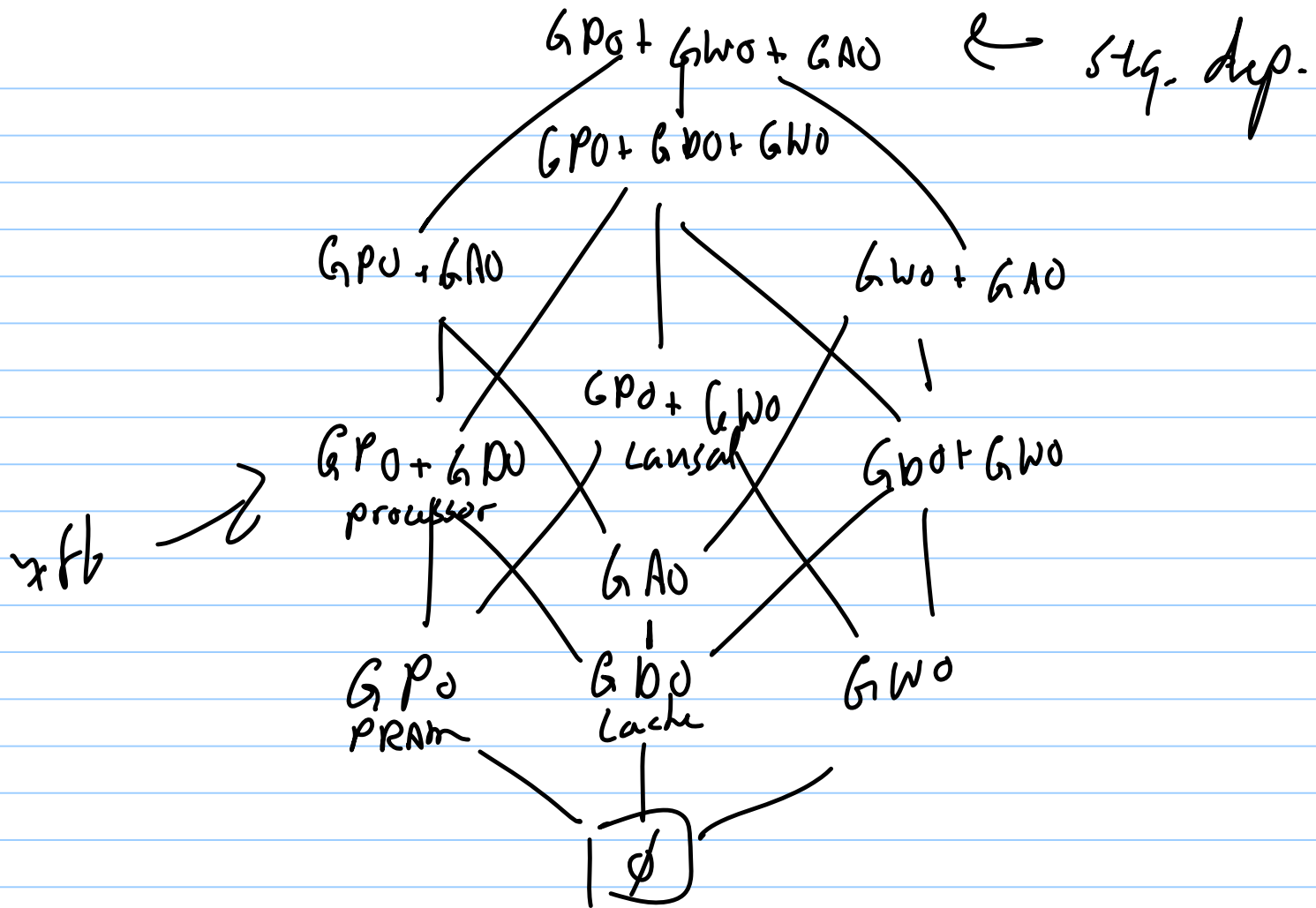
view - what is the process' view of order of events

PRAM consistency "pipelined RAM"

- must see ops to occur in program order
- diff procs may see diff orders

"programmer's view" is important





## synchronized consistency models

have explicit sync actions and/or variables

- weak consistency

- access to sync variables are seq. consistent

- access to " " " is in known order relative to all other variables



