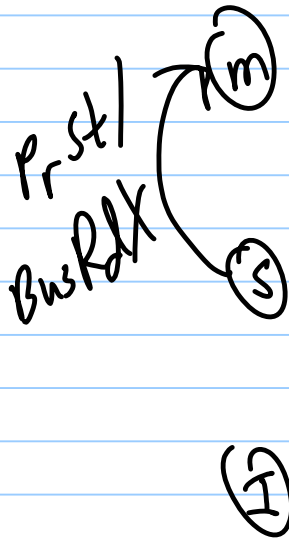
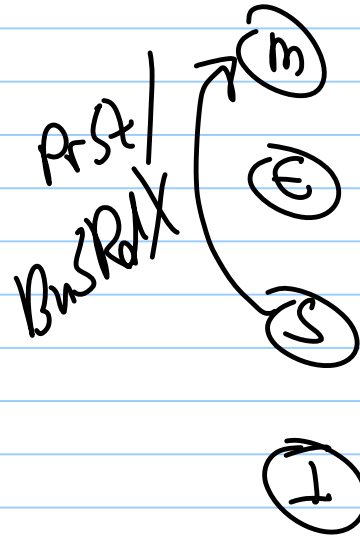


# Cache Coherence (cont.)

MSI



MESI



Bus Upgr  
BusRdX w/o  
data movement

update protocol

Dragon Write-back Update Protocol

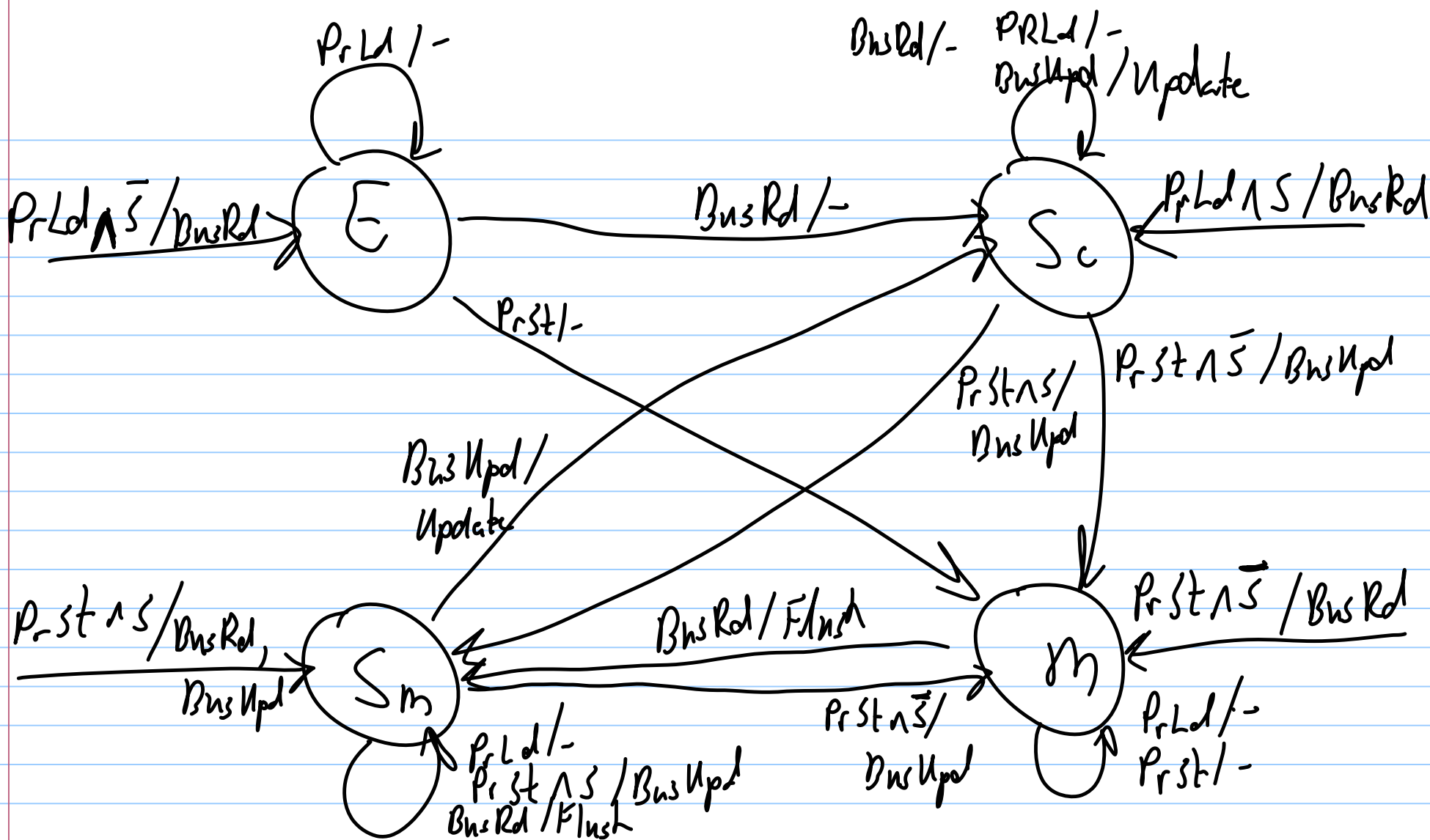
4 states

E Exclusive Exclusive clean  
I and memory have block

S<sub>c</sub> Shared clean  
I, others, maybe memory have block  
but I'm not owner

S<sub>m</sub> shared modified  
I, others, but not memory have block  
I am owner

M I and no one else have block



## Token Coherence

protocol invariant

each memory block has either multiple  
read-only copies or a single writeable copy  
XOR

MSI & variants use interacting FSMs to enforce

TC counts explicit tokens

1 needed to read  
all " " write

## mechanisms (2)

- token counting

$T$  tokens, in memory,  
in cache, or in msg

4 rules

1. At all times, exactly  $T$  tokens exist, 1 is owner
2. A proc. can write to a block only if it has  $T$  tok,
3. " " " " " " " "  $\geq 1$  tok
4. If a coherence msg contains the owner token,  
it also contains valid data.

persistent requests / timeout, e.g.

upon detection of potential starvation  
initiate pers. req.

1 pers. req. is allowed per block  
this triggers all tokens to go to requester

see Fig 2 in Martin, Hill, Wood