

# Coherence Protocols

Note Title 2/24/2009

## Invalidation protocols

bus xaction      Read-exclusive

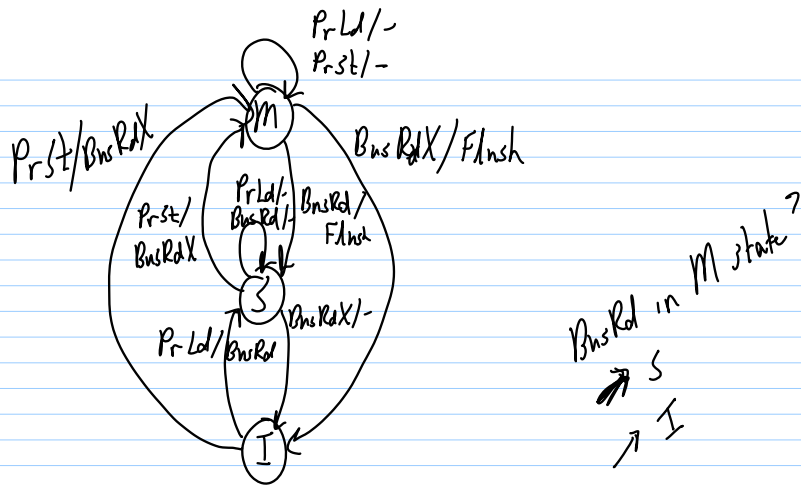
## Update protocols

bus xaction      Update

## Basic MSI Protocol

M - modified / dirty  
 S - shared - one or more proc.  
 I - invalid

proc events	load	PrLd
	store	PrSt
bus events	BusRd	read
	BusRdX	read-exclusive
	BusWB	write back

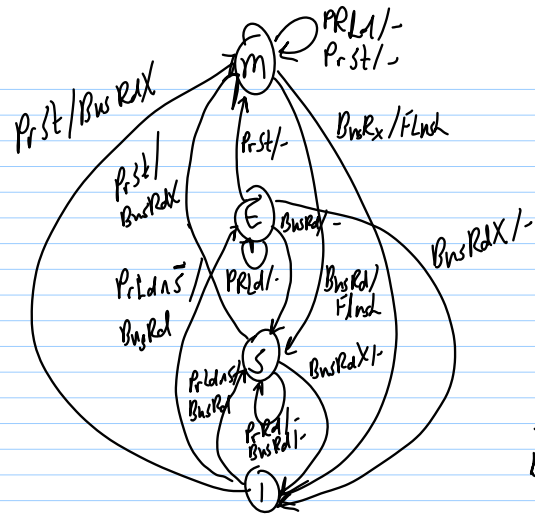


## MESI 4-state protocol

Add exclusion state E  
 proc has only cached copy  
 it is still clean

I → E      PrLd if no one else has copy

Illinois



PrLdA S  
I → S

PrLdA S  
I → E

S says whether a  
BusRd results in a  
shared state

## MOESI

AMD

0

Owned

most recent data

others may share

main memory may be stale  
responsible for providing data

only 1 proc in 0 state