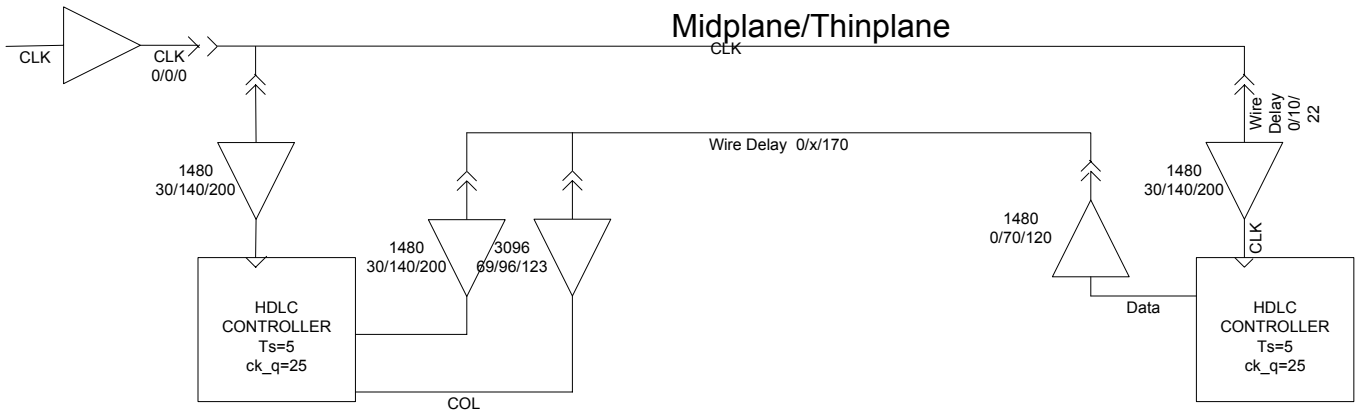


# HDLC CLK/DATA TIMING ANALYSIS

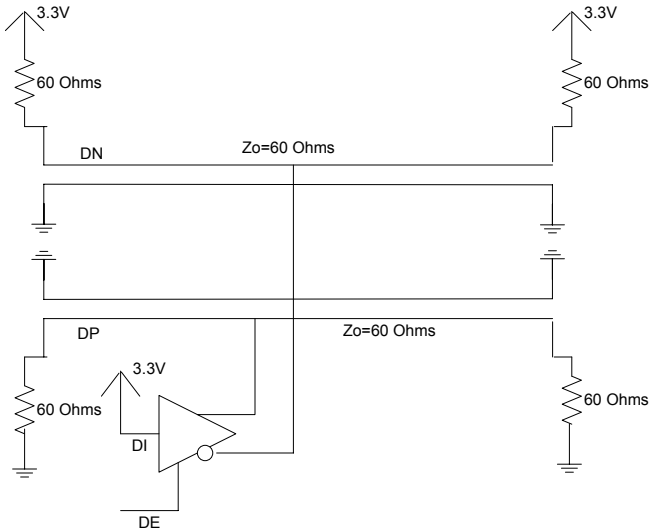


Card A

Card B

xx/xx/xx indicates min/typ/max delays in ns. For wires it is the total delay of that wire, for logic components it is the delay in that component

Clock is 1 MHz, 50% duty cycle, data values are stored on rising clock edge, outputs updated on falling clock edge. Thus, hold is no problem but setup may be.



DU is data input, DE is enable. Enable is driven high to put H level on the DP/DN differential pair