EE464
Digital Systems Packaging

Spring, 2003

Fred U. Rosenberger
EE Dept, Washington University
fred@cse.wustl.edu

Chapter 1 of Text

- Why?
  - It's there
  - Cover in order
  - Future/Trends/What-Next
  - Environment for our systems
  - What is possible/practical depends on the physical characteristics of connections (wires)

What is Packaging?

- Connections (wires and conductors)
- Isolation (insulators, space, shields)
- Power distribution
- Mechanical support
- Cooling

Wires/Conductors

- Metal (almost exclusively)
  - » Al (Aluminum)
    - – Best conductor by weight and cost
    - – Used for smallest conductors (ICs) for mechanical properties
    - – Used for the largest conductors (for power because of cost)
  - » Cu (Copper)
    - – Used at many intermediate levels (package, PC board, wire)
    - – Solders well, important to PC-level and wire interconnect
    - – Solder or pressure (gas-tight) required to prevent oxidation
    - – Now used in ICs for lower resistance
  - » Au (Gold)
    - – No oxidation, good for connectors/contacts/oxide-free plating
  - » Ag (Silver)
    - – Best conductor by volume
    - – Used for some high-current contacts
    - – Silver sulphide forms over time, very bad

Wires/Conductors (Continued)

- Metal (almost exclusively)
  - » Tin
    - – Inexpensive plating for solderability and contacts
  - » Nickel or Palladium
    - – Used for Barrier between copper and gold (copper will diffuse through gold plating)

Isolation (and Mechanical Support)

- Silicon Dioxide (ICs)
- Fiber-glass epoxy (PC boards)
- Teflon
- Polyethelene
- Other plastic like materials
- Air

Power, Cooling, Mechanical Support

- Power, cooling, and mechanical support are all necessary
- Sometimes handed off to MEs but tradeoffs abound
- Stiffners, heatsinks, fans, …

Packaging Levels

- IC Chips
- Packages and MCMs (MultiChip Modules)
- PC Boards
- Backplanes
- Chassis (shelf)
- Rack
- Room
- Building
- World

Increasing Density of Connections

- Wire-wrap: a technology that has come and gone
  - » gas-tight connection
  - » Does not scale well to high-density
- Smaller dimensions
  - » 0.1, 0.05, 0.025 inch lead spacing on PC boards
- New configurations
  - » DIP (Dual In-Line) not very efficient, Obsolete
  - » Surface mount
    - – no vias required
    - – Components on two sides of PC board, very dense
  - » 2-D arrays of pins/balls (PGA, BGA)
  - » MCMs, stacked, …

Why does everything get smaller?

- Its possible
- Its necessary
- Example: Cray
  - » Circular arrangement of racks
  - » Cray 4 with thinned chips and robotic assembly
- Transition time to connection length
  - » tr>>length: easy (length approx 2ns/ft
  - » Ethernet

Why does everything get smaller (Continued)?

- Why I/O density
  - 16, 64, 256, 1024, 2048 connections/package
  - Alternative is fewer but faster (or both)
  - Increasing logic speed
  - Memory-Processor bottlenecks
  - Communication in general

Cost

- Photographic techniques allow many connections to be fabricated with few steps (relatively cheap)
  - » ICs
  - » PC boards
  - » Fewer errors than individual wires
    - – connection points
    - – poor solder or workmanship
- Connectors are expensive and limiting
  - » Faults and defects
  - » Inductance and coupling

From Table 2-1 in Text Properties of Packaging Levels

Level	Size	Layers	Pitch (um)	Tracks/ Layer	Wire Cross Section (um)	R (Ohm/ mm)	Wire Model	C (pF/mm)	Pins
Chip	15x15 mm	4	1.2	12,500	0.6x0.6	150	C/RC	0.2	500
Package	5x5 cm	4	150	333	75x20	1 (Total)	LC	1 pf (Total)	500
PC board	40x30 cm	8	625	2000	125x20	0.05	LC/LRC	0.1	2000?
Backplane	40x30 cm	8	625	2000	125x20	0.05	LC/LRC	0.1	1000
Chassis	40x40x40 cm	N/A	N/A	N/A	N/A	N/A	LC/LRC		1000
Cabinet	1.5x.6x.6 m	N/A	N/A	N/A	N/A	N/A	LC/LRC		3000

Notes

- R is a function of absolute dimensions
  - » Small geometries have large R (rho(L/WT)
- C and L are a function of ratios, not absolute diminsions
  - » C and L are approximately the same for all levels of packaging
  - » C for chip level is a little higher because of adjacent signals
  - » Really crude rules of thumb
    - C=4 pF/inch 1.6 pF/cm
    - L=10 nH/inch 4 nH/cm

IC Package Parasitics, BGA

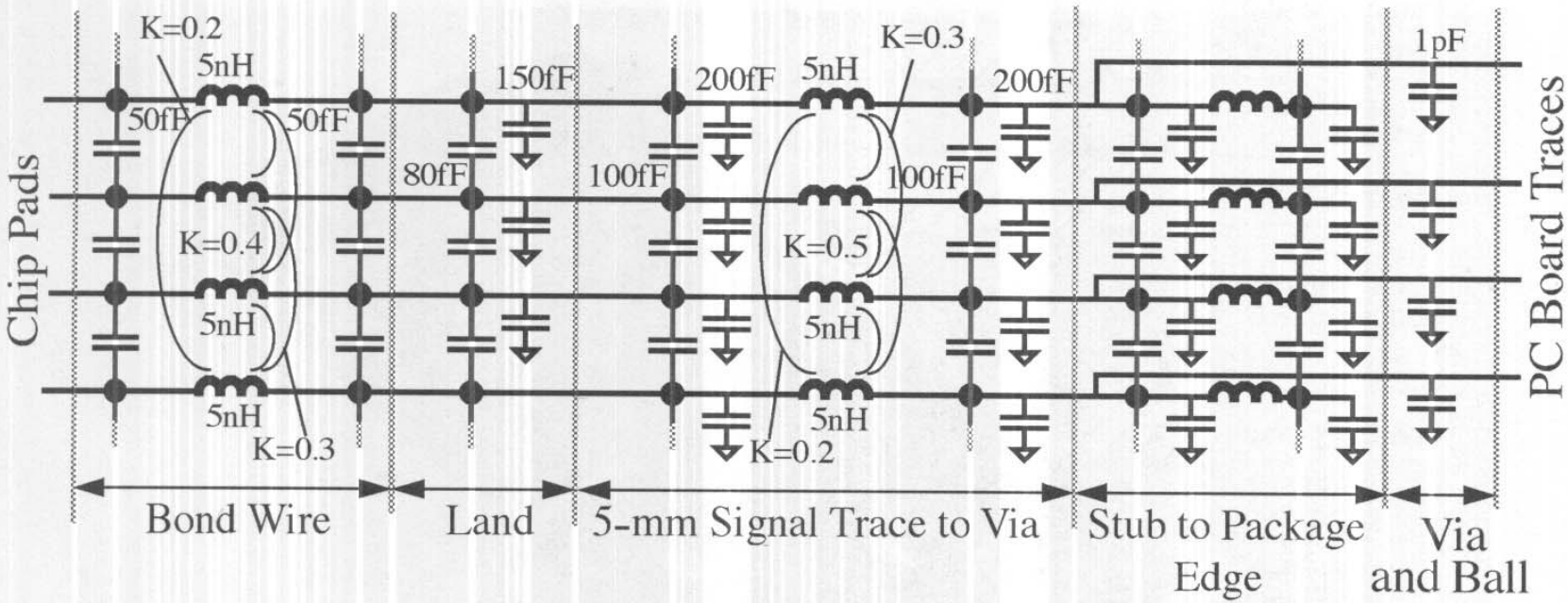

FIGURE 2-11 Package Lumped-Element Model

Trends/Directions

- Smaller
  - » Because we can
  - » Faster
  - » Shorter connections
  - » Less power
- More integration
  - » Termination resistors built-in PC board
    - – To be superceded (or concurrently) by termination resistors in ICs (better)
  - » Capacitors built-in PC board (at least highest frequency)
    - – To be replaced/augmented by capacitors built-in ICs/Packages?
- Elimination of packages
  - » Wasted volume, lead length, etc
- MCMs? (minature PC boards with multiple chips)
  - » Additional levels of packaging?
  - » MCMs on MCMs on PC boards on PC boards on …
  - » Presently have packages on daughter boards on PC boards in chassis …

Trends/Directions (continued)

- Smaller sizes, denser, more pins
- Serial transmission (only way to get really high data rates because of skew)
- Differential transmission
  - » Balanced, zero net current
- Point to point (perhaps with switches) rather than busses
- Lower voltages
- Every off chip connection will be a transmission line
- DC-DC converter for each (large) IC?
- Reduction/elimination of glue logic?
  - » Programmable devices/interfaces