Noise Margin Definition
(from JEDEC Dictionary)

- Noise margin: The maximum voltage amplitude of extraneous signal that can be algebraically added to the noise-free worst-case input level without causing the output voltage to deviate from the allowable logic voltage level.

  NOTE The term "input", as used here, refers to logic input terminals, power supply terminals, or ground reference terminals.

- How do we apply this?

Noise Margin: Allows digital circuits to propagate signals through any number of elements without error

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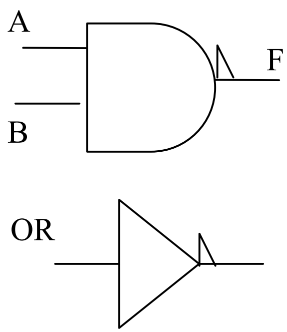


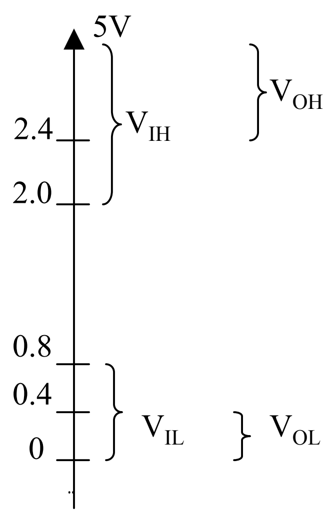
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

A	B	F
L	L	H
L	H	H
H	L	H
H	H	L

What does this mean?

L = ?

H = ?



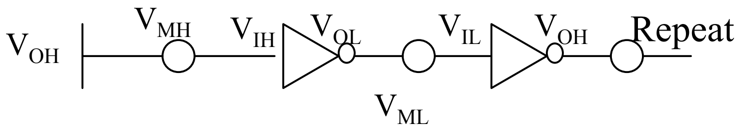
$V_{MH} = V_{OHMIN} - V_{IHMIN}$

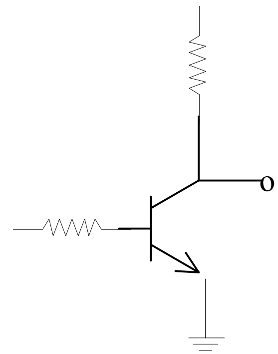
$V_{ML} = V_{ILMAX} - V_{OLMAX}$

V_{IHMIN}	2V
V_{OHMIN}	2.4V
V_{ILMAX}	0.8V
V_{OLMAX}	0.4V
V_{OLMAX}	Max Output V
V_{ILMAX}	Max Input V, That is L for all

Agreement or Contract

For all (bounded, ignore random/real noise) conditions (T, V_{dd} / V_{cc}, load, age, other inputs, …), truth tables satisfied if voltages in range.

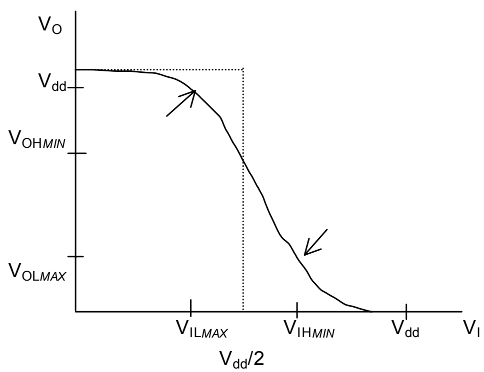


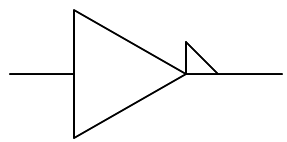


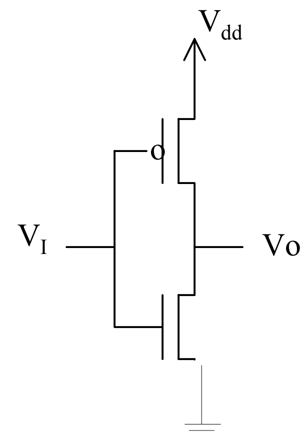
What about $V_{IH\,MAX}$, $V_{IL\,MIN}$?

Usually just damage but can effect output.

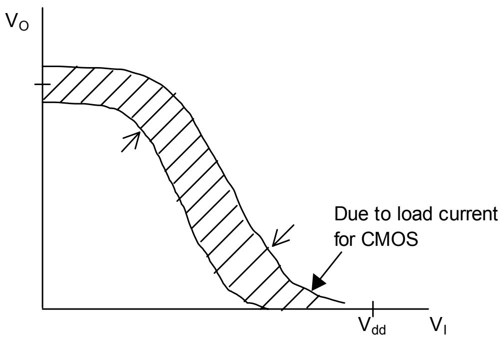
Transfer Function



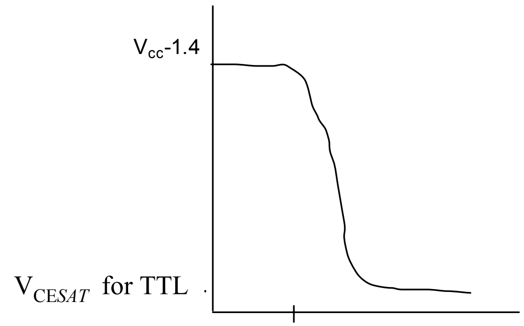


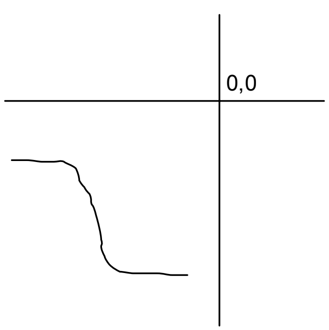


We (manufacturer) can choose specification points (and test)

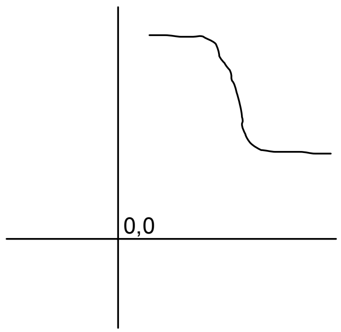


TTL

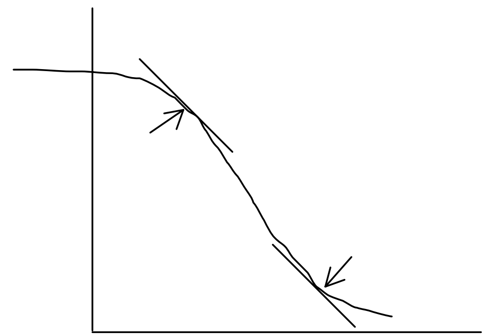




OR

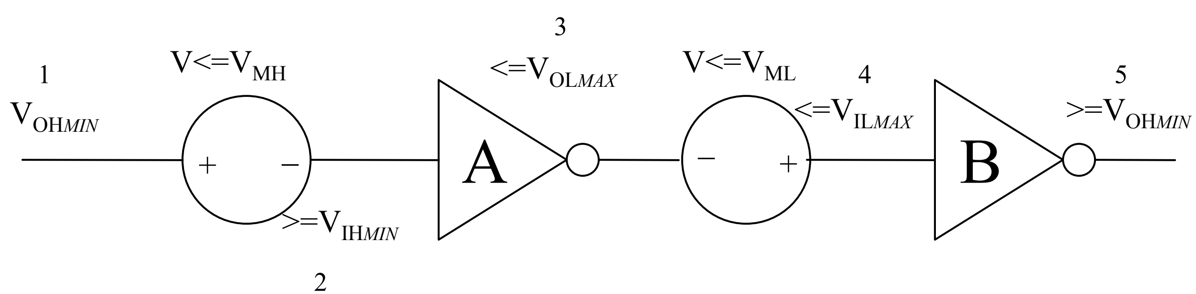


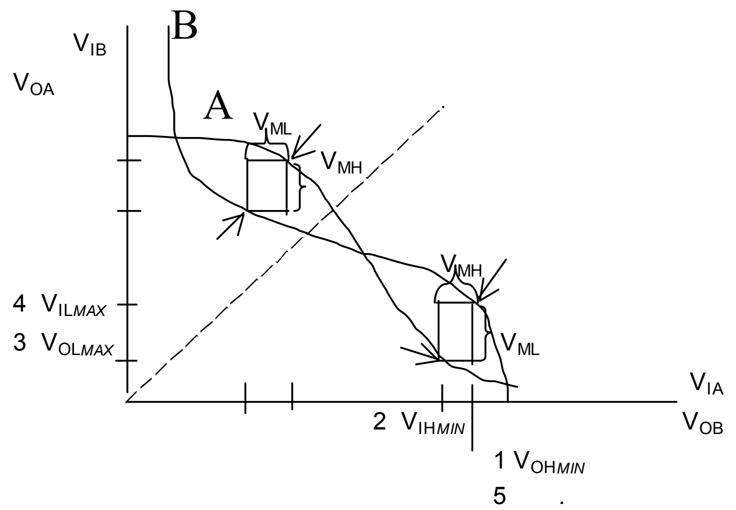
Typical electronics textbook (Sedra & Smith) says: “Choose specification points at gain = minus 1”.



This maximizes $V_{MH} + V_{ML}$.
For symmetric transfer characteristic it is best, but may not be best for non-symmetric.
e.g.: Could have V_{MH} = 2V, V_{ML} = -1V, Vsum = 1V.

Usually want to maximize the smaller (unless we want something else (impedance?)).

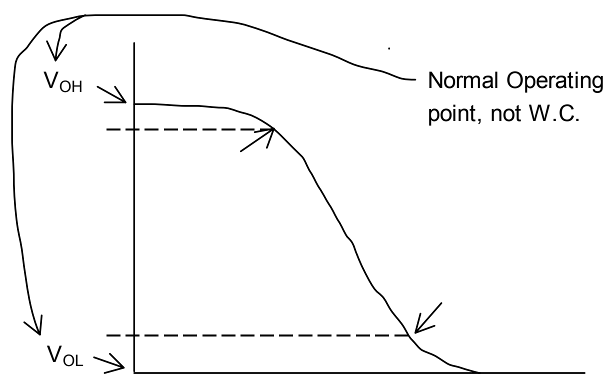




Maximum square gives max smallest V_M (& Equal). If symmetric it is at unity gain points.

We need |Gain| > 1 and overlapping region (Can get by level shifting).

Most texts use (wrong):



Gives Larger noise margin def.

Does not allow noise at every node.

No design rule can be derived.

(Here noise = 0 at all but one node? NO!)

Our text has different orientation/emphasis: noise immunity. V_M/Vswing

V_M is directed toward simplest gates. Lots of logic, short connections.

Text is oriented to smaller number of longer connections where noise is greater and more components (FETS) can be used. Also oriented toward design (choose Vswing)

Which is better?

A	B	C
$V_{MH} = 1V$	$V_{MH} = 0.5$	$V_{MH} = 0.4$
$V_{ML} = 0.8V$	$V_{ML} = 0.5$	$V_{ML} = 0.3$

Naturally it depends!: what is max signal swing (V_{OH}-V_{OL}), what is source of noise.

Figure of merit is V_M/signal-swing (larger is better, 0.5 is best possible)

Other

- Max input High, Min input Low: damage, incorrect operation?
- Generally expect, *monotonic* transfer characteristic, positive resistance, not always true
- Output and Input currents must be considered, V_M may apply only over some range of loads (essentially infinite for CMOS, 10 for 7400)
- Non-inverting logic elements
- V_M applies to a system of logic elements, not to a single element, although we refer to the V_M of a logic element
- Most noise is internally generated, not external so V_M /signal-swing Noise Immunity, not absolute value of V_M is almost always most important.
- Large asymmetry in transfer characteristic can be bad, large noise generation with small noise margin
- AC noise margin is *typically* greater than DC
- V_{IHmin} for a set of logic elements? Largest V_{IHmin} in the set!
- "Clever circuits" sometimes have "clever failure modes"
- TTL(74,74L,74H,74S,74LS,74ALS,74AS)/RTL/DTL/CMOS/ECL/PECL/CML/GTL/GTL+/BTL/HSTL/SSTL/LVDS/…

Fundamental

- If noise is less than noise margin, digital signals can propagate through an infinite number of elements and remain error free
  - Assuming fault-free components
  - Very good approximation at present, will not hold as voltages decrease and “random” noise becomes more important, not true at present in some high-speed systems, or in magnetic recording.
- A major goal of signal-integrity or high-speed design or digital systems engineering is to maintain noise amplitude less than noise margin during critical times (sampling times)
  - Minimize noise (or: small enough)
  - Maximize signal (or: large enough)
  - All with acceptable (or optimum) power dissipation, delay/speed, component count, design time, …
  - Some systems aim for acceptable error rate, rather than error free
  - At the fundamental level of operation, digital circuits are analog, and must be analyzed as such. “Digital” is a convenient model or abstraction
  - Be careful with “textbook” definitions: spec points, slope= -1