
EE273 Lecture 13

Clock Distribution

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Logistics

- Reading
 - Sections 10.1 and 10.2
 - Complete before class on Monday 3/1
- blank pages in back for notes

How are people doing on their projects?

A Quick Overview

- The clock-distribution problem
 - want lots (10^5 - 10^8) of clock loads to see the clock rise at precisely the same picosecond
 - noise and variations in delay of distribution network make this difficult
- Clocks are different than signals
 - We can exploit this difference
- Off-chip Clock Distribution
 - wires are good LC transmission lines
 - typically use a tree of clock buffers
- On-chip Clock Distribution
 - wires are slow RC transmission lines
 - buffer delay is modulated by power-supply noise
 - still use a clock tree, but concerns are different

The Clock Distribution Problem

- Some systems have large synchronous clock domains
 - 10s - 100s of chips
 - 10^3 - 10^5 clock loads per chip
 - need to distribute the clock to within 10% of t_{ck}
 - 200ps for a 500MHz clock
- Two step process
 - get the clock to each chip with low skew
 - distribute the clock on each chip with low skew
- Other issues
 - may not want a single point of failure
 - can't have just one clock oscillator or master buffer
 - need to adjust for manufacturing variations with a minimum of labor

Off-Chip Clock Distribution

- Relatively easy because wire delays are
 - stable
 - easily characterized
- Most common strategy is a clock tree
 - single oscillator
 - buffer tree with a fanout of N
 - low-skew fanout buffers used
 - e.g., Motorola 100LVE111
 - tuning needed to get very low skews
 - self-tuning series terminated drivers
- For fault tolerance can use an array of oscillators
 - phase lock multiple clock generators to one another
- Traveling waves and standing waves can also be exploited
 - round-trip clock distribution
 - salphasic clock distribution

A Typical Clock-Tree Driver The 100LVE111

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Low-Voltage 1:8 Differential ECL/PECL Clock Driver

MC100LVE111

LOW-VOLTAGE 1:8 DIFFERENTIAL ECL/PECL CLOCK DRIVER

The MC100LVE111 is a low-voltage 1:8 differential driver designed with clock distribution in mind. The MC100LVE111's function and performance are similar to the previous MC100LVE110, with the added feature of low-voltage operation. A tri-state output signal when one or other differential output is not needed is added to allow the signal to be turned off to a differential differential output.

- 20kVc Part-to-Part Bias
- Noise-Insensitive Output Stages
- Differential Output
- High Output
- Voltage and Temperature Compensated Outputs
- Low Voltage V_{CC} Range of 0.9V to 1.8V
- PECL Input/Pullup Function

The LVE111 is specifically designed, modeled and produced with low skew and low jitter. Output design and layout rules to minimize gate to gate skew within a device and empirical modeling is used to minimize gate to gate skew. The device is designed to minimize gate to gate skew. To ensure that the right skew specification is met it is required that both sides of the differential output are terminated into 50Ω and if only one side is being used in most applications, all non-differential pairs will be used and therefore terminated in the case where there are two pairs available. It is required to terminate all unused pairs in the same manner as the pairs being used. In the case of one or two pairs being used, pairs to be left will match small impedances of parasitics along the line or the other side of the signal being used which, while not being catastrophic in most designs, will mean a loss of skew margin.

The MC100LVE111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE111 to be used for high performance clock distribution in CMOS systems. Careful use like arrangement of the LVE111's connections is required to allow correct PECL operation. In PECL mode, the LVE111's performance is typically not as good as in differential mode. For systems requiring 50Ω parallel termination after the driver, care should be taken to ensure the V_{CC} supply is a terminating voltage. For more information on using PECL, designers should refer to Motorola Application Note 600-0300.

AS A NOTE
PARTS PACKAGE (GDSI 176-02)

MC100LVE111

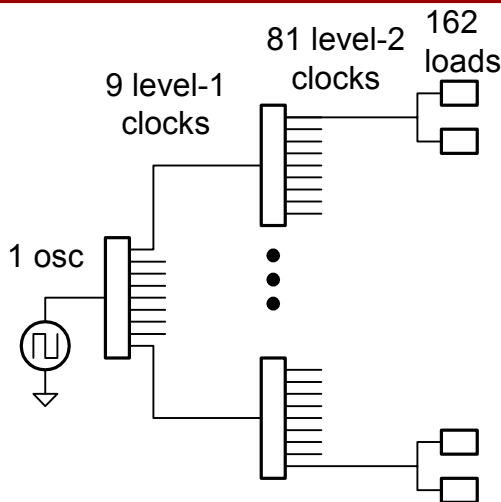
Pin Name	Function
Pin 1	Reference
Pin 2	Reference
Pin 3	Reference
Pin 4	Reference
Pin 5	Reference
Pin 6	Reference
Pin 7	Reference
Pin 8	Reference
Pin 9	Reference
Pin 10	Reference
Pin 11	Reference
Pin 12	Reference
Pin 13	Reference
Pin 14	Reference
Pin 15	Reference
Pin 16	Reference
Pin 17	Reference
Pin 18	Reference
Pin 19	Reference
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Pin 90	Reference
Pin 91	Reference
Pin 92	Reference
Pin 93	Reference
Pin 94	Reference
Pin 95	Reference
Pin 96	Reference
Pin 97	Reference
Pin 98	Reference
Pin 99	Reference
Pin 100	Reference

Pinout: 80 Lead PLECC (Pin 100)

LOAD SYMBOL

Skew:
50ps within a part
200ps across parts

An Example Clock Tree



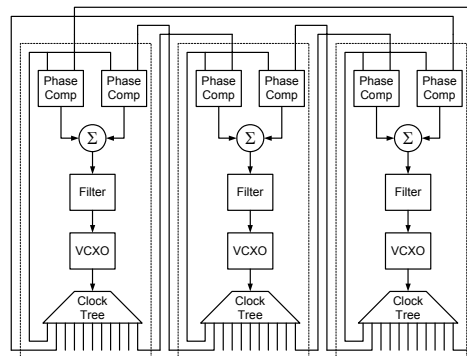
All lines are
differential and
terminated into 50Ω

Clock Trimming

- If open-loop skew is not good enough, clocks can be *trimmed*
 - adjust the *length* of each fanout to equalize delay
 - trombones
 - RC padding
 - modulation of buffer delay
- This can be done manually or automatically

Coupled Oscillators

- Avoid single point of failure
- Average phase of several clocks



Salphasic Distribution

- Drive an unterminated (or shorted) line with a sine-wave
- Standing wave has the same phase everywhere
 - just different amplitude
- Amplify and limit this wave to generate a clock with negligible skew!

$$V_f(x, t) = \sin(\omega t + \theta - x/v)$$

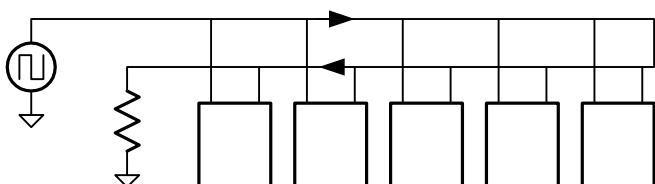
$$V_r(x, t) = \sin(\omega t + \theta + x/v - 2l/v)$$

$$V = V_f + V_r = 2 \sin(\omega t) \cos\left(\frac{x-l}{v}\right)$$



Round-Trip Distribution

- Send clock down an array of modules (e.g., a bus) and back
- Each module sees forward and reverse traveling clock
- The average time of arrival is the same for all modules
- Modules can interpolate the forward and reverse traveling clocks *or*
- Data can be sent forward with the forward clock and backward with the reverse clock

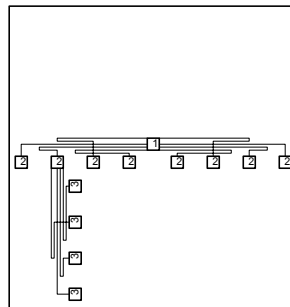


On-Chip Clock Distribution

- A large ASIC may have 10^4 to 10^5 clock loads
- Each is about 20fF
 - total load is 200pF to 2nF!
 - this load switches every cycle
- Need to
 - amplify a small clock signal to drive a 2nF load
 - distribute the clock over resistive wires to the amplifiers and loads
 - repeaters needed on long runs
 - avoid jitter
- Jitter comes from 3 main sources
 - differential supply variation modulates the delay of the clock buffers
 - single supply variation modulates the thresholds of the clock buffers
 - crosstalk to adjacent lines changes the delay of the clock fanout lines
- Each of these sources can be dealt with

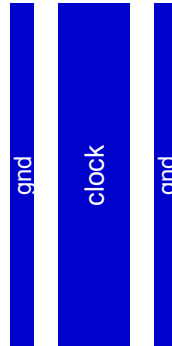
An On-Chip Clock Tree

- Distribute clock from center of chip
- Fanout first in X, then in Y
 - H-tree layout also possible
- Line lengths balanced at each stage of fanout
- Repeaters needed in long lines
- Wider than minimum width lines usually used
- Adjacent ground shields to eliminated crosstalk
- Differential distribution to avoid threshold shift
- Buffer sizing adjusted to match delay to varying spatial load



Reducing Jitter

- Address each of the three sources
- Differential Supply Noise
 - use a separate 'clock' power supply
 - adequately *bypass* this supply on chip
 - use insensitive buffers
- Single Supply Noise
 - use differential signaling
- Crosstalk
 - surround clock lines by parallel *shields*



Clock Grids

- Tie points of clock distribution network together in a grid
- Averages phases of nearby regions
- Performance depends on RC time constant of grid
- Need to avoid supply overlap current

On-Chip Clock Trim

- Can locally adjust the phase of clock drivers to compensate for
 - Load variation
 - Process variation in distribution network
- Adjust via
 - Phase locking local oscillators
 - Trimming variable delay

Next Time

- Synchronization

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