
EE273 Lecture 12

Closed-Loop Timing

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Logistics

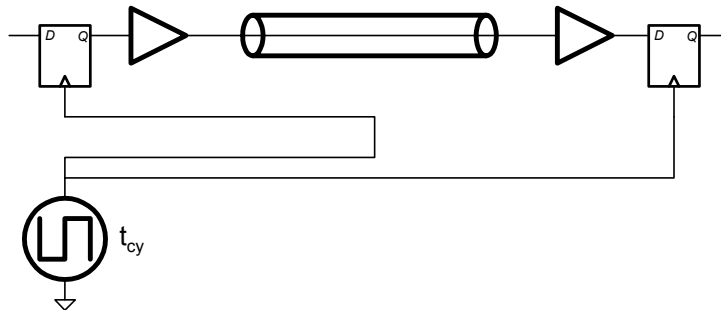
- Reading
 - Section 9.7
 - Complete before class on Wednesday 2/25

A Quick Overview

- Pipeline timing
 - forward clock with the data
 - eliminates 'windows' of operating frequencies
 - system works from DC to maximum frequency
- Closed-Loop Timing
 - skew can be eliminated by
 - measuring it
 - adding delay to compensate
 - example: a zero-delay buffer
 - phase comparator
 - variable delay line
 - components
 - phase comparator
 - variable delay line
- Bundled closed-loop timing
 - timing loop closed around one reference line
 - most sources of skew uncompensated
 - depends on matching of reference and data lines
- Per-line closed loop timing
 - timing loop closed individually around each data line
 - most sources of skew compensated

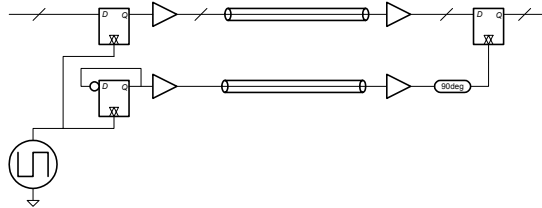
Synchronous Timing

- Same clock used at both ends of the line
- Operates in narrow frequency ranges each centered on $k+0.5$ bits on the line for integer k .



Pipeline Timing

- Delay the clock by the same amount as the data *plus* half a bit cell
- System will work from DC to maximum frequency $1/(t_r+t_a+t_u)$
- Defines a new clock domain at the far end of the line

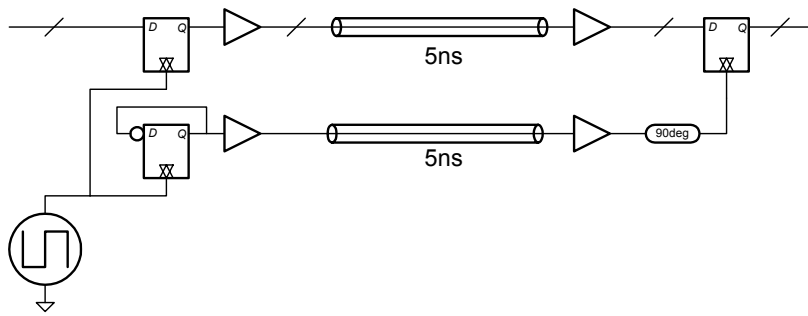


Pipeline Timing Example

$t_r=100\text{ps}$, $t_a=50\text{ps}$

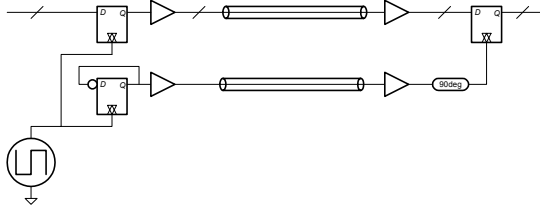
$t_j=10\%$ of active delay, $t_s=10\%$ of active delay, 1% of wire delay

$t_{dCQ}=200\text{ps}$, $t_{\text{buf}}=200\text{ps}$, $t_{\text{clk_buf}}=600\text{ps}$



Sources of Timing Uncertainty

- Skew
 - between clock line and data line
 - fixed differences in flip-flop, transmitter, and receiver delays
 - in transmit clock between flip-flops
 - aperture offset in receive flip flop
 - offset in 90 degree delay line
- Jitter
 - in transmit clock
 - in delay of flip-flops, transmitters, and receivers

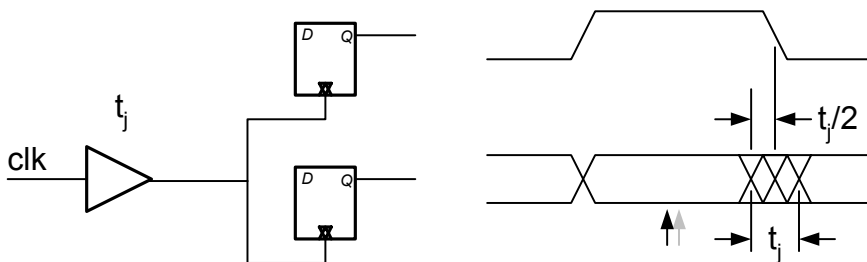


Sources of Timing Uncertainty

Element	Quan	Delay	Skew	Jitter
Clock Buffer	0.5	600	0	30
Tx FF	2	200	40	40
Tx Driver	2	200	40	40
Line	2	5000	100	0
Rx Receiver	2	200	40	40
TOTAL			220	150

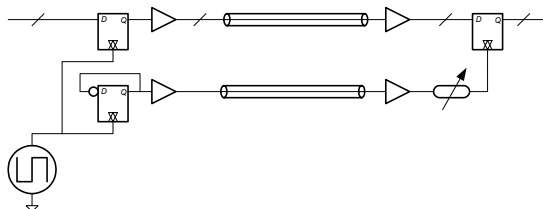
$$t_{\text{bit}} \geq 100 + 50 + 370 = 520$$

Common Path Jitter

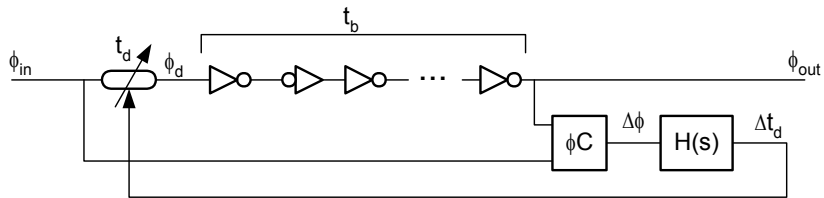


Closed-Loop Timing Measure and Cancel Skew

- All skew can be canceled by a variable delay element
 - in clock or data path
- Delay line is adjusted to center the clock on the eye
- To adjust the delay, need to *measure* the timing
 - Usually an iterative process, measure-adjust-measure...



Example, a Zero-Delay Clock Buffer

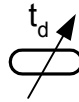


Timing Loop Components

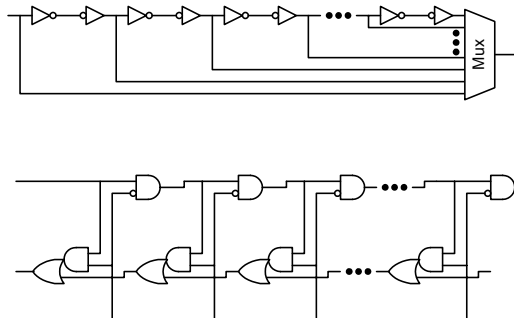
- Phase Comparator
 - measures the time difference between two signal transitions
 - for periodic signals measures the phase of one signal with respect to the other
 - the sensor for most timing loops
- Delay Lines
 - adjust the delay between two points in a system
 - the actuator for most timing loops
 - except for PLLs that use VCOs
- Loop Filters
 - smooth response of the timing loop
 - stabilize the loop (for PLLs)

Variable Delay Lines

- Need:
 - a delay element
 - a method to vary the delay
- Delay elements
 - inverter
 - source-coupled amplifier
- Methods to vary delay
 - multiplexing a tapped delay line
 - varying the power supply to an inverter chain
 - varying the capacitance driven by each stage
 - varying the resistive load of a source-coupled amplifier
- Characterized by
 - max and min delay
 - typically a 2:1 throw
 - stability (jitter)

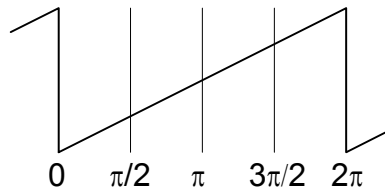
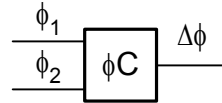


Some All Digital Variable Delays



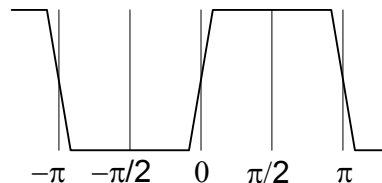
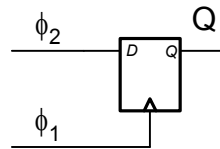
Phase Comparators

- Output describes phase difference between two inputs
 - may be analog or digital
 - may linearly cover a wide range, or just a narrow phase difference



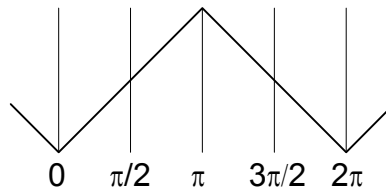
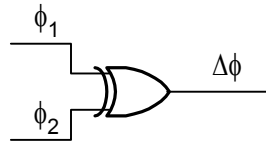
Flip-Flop Phase Comparator

- Feed ϕ_1 into the clock input
- Feed ϕ_2 into the data input
- With single-edge triggered FF, if Q is low, ϕ_1 is (early late) (circle one).
- How does this work with a double-edge-triggered FF?
- Note that when $\Delta\phi = 0$, FF is put in a metastable state
- If same FF used for receiver and phase comparator, aperture offset is compensated for.



Exclusive-OR Phase Comparator

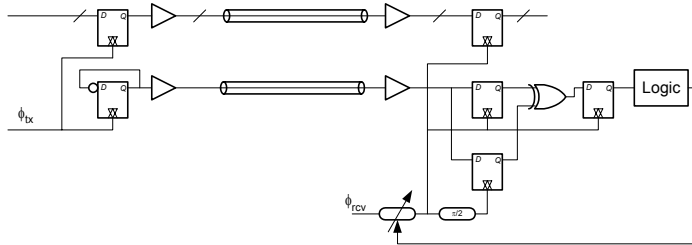
- Duty factor out of comparator is proportional to phase
 - requires a low-pass filter to extract a usable value
- Wide linear range allows locking to $\pi/2$
 - but low gain implies large jitter. Small voltage noise gives big phase noise.



Other Phase Comparators

- Sequential phase-only comparator
 - asynchronous state machine
 - pulses “up” or “down” output from transition on one input to transition on the other
- Sequential phase-frequency comparator
 - like the sequential phase-only comparator
 - but also keeps track of number of transitions on the two inputs and attempts to make them equal
 - don’t use this for a DLL!!!

Link with Bundled Closed-Loop Timing



Which of these elements of timing uncertainty are cancelled?

- Skew
 - between clock line and data line
 - fixed differences in flip-flop, transmitter, and receiver delays
 - in transmit clock between flip-flops
 - aperture offset in receive flip flop
 - offset in 90 degree delay line
- Jitter
 - in transmit clock
 - in delay of flip-flops, transmitters, and receivers

Next Time

- Clock Distribution