
EE273 Lecture 9

Off-Chip Power Distribution

February 9, 2004

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Logistics

- Reading
 - finish Chp. 5
 - Complete by Wed 2/11
- Midterm
 - Wed, 7PM to 9PM.
 - room: in the Quad, Bldg. 420, Room 041
 - for directions, see last lecture
 - will cover through advanced signalling (not power)

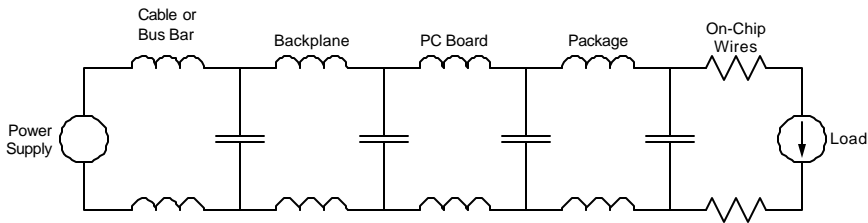
A Quick Overview

- The Power-Distribution Problem
 - DC supply voltage with small tolerance
 - AC current, large di/dt
 - Inductive and resistive supply components
- Inductive Power Supply Noise
 - L supplies low-frequency current, C supplies high frequency
 - ripple due to current variation within each cycle
 - transient at start/stop of load current
- Bypass Capacitors
 - parasitic L and R in capacitors make them effective only below a certain frequency
- Local Regulation
 - series and parallel (shunt)
 - clip voltage ripple
 - 'subtract' AC current
 - distribute at a more convenient voltage

The Power Distribution Problem

- Modern digital systems operate at small DC voltages
 - 1.2 to 3.3V
 - must be held to within $\pm 10\%$ (or less)
- and draw large AC currents
 - 10A or more per chip, 100A per board, KA in a system
 - may go from 0 to full current in less than one clock cycle
- over a supply network with parasitic elements
 - Inductance of bus bars, PC boards, packages, and bond wires
 - Resistance of on-chip wires

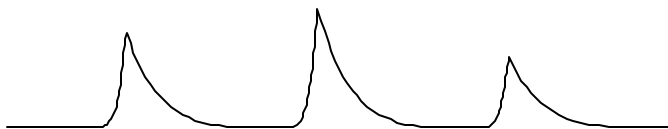
A Typical Power Supply Network



- Actually a tree with branching at each level
- Parasitic inductance (off-chip) and resistance (on-chip)
- Power and ground networks are usually symmetric
- Capacitance added to give a *tapered* frequency response

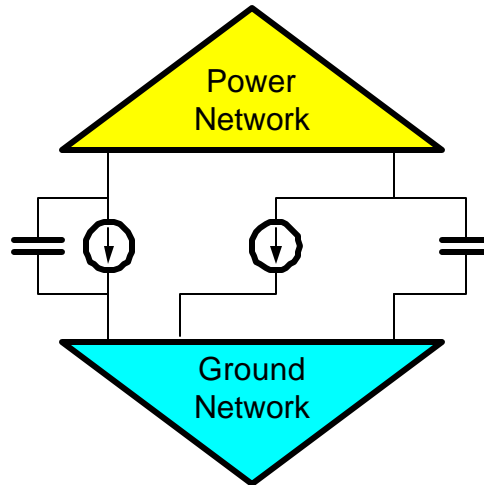
Typical Load Current

- For a given clock domain, load is usually periodic with the clock
- May stop or start in a single clock cycle
- With multiple clock domains, they may drift into phase reinforcing one another
- Load is often *resistive*, varying linearly with supply voltage
- Some loads are *high impedance*, constant independent of supply voltage



Local Loads and Signal Loads

- Logic loads connect a point in the power network to a corresponding point in the ground network
 - current can be supplied from a nearby bypass capacitor
- Signal loads connect a point in the power network to a distant point in the ground network
 - usually due to unbalanced signaling
 - current must return over a long path
 - bypass capacitors are not effective



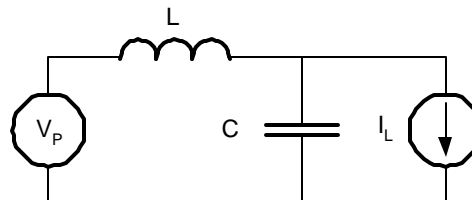
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Inductive Supply Noise

- Each section of the supply network is an LC circuit
 - has a resonant frequency, $\omega_{LC} = (LC)^{-1/2}$
 - inductor carries DC current ($\ll \omega_{LC}$)
 - capacitor supplies AC current ($\gg \omega_{LC}$)
- Size capacitor to
 - supply cycle to cycle AC current with acceptable ripple
 - handle inductor start/stop transient

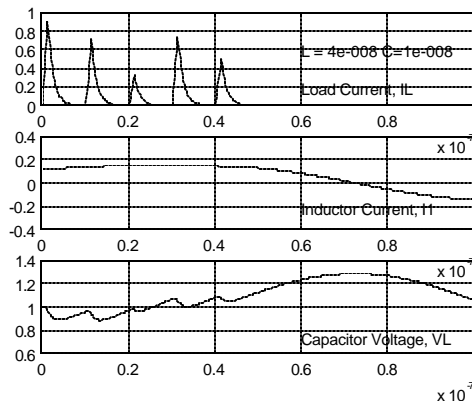


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Response of an LC Section to Typical Supply Current



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Magnitude of Ripple within a Cycle

- Over a clock cycle, inductor current is essentially constant, I_{avg}
- Load current varies considerably
- Capacitor current is the difference
- Capacitor voltage *ripples* due to this AC current

$$\Delta V = \frac{k_i I_{\text{avg}} t_{\text{ck}}}{C_B}$$

$$C_B > \frac{k_i I_{\text{avg}} t_{\text{ck}}}{\Delta V_{\text{max}}}$$

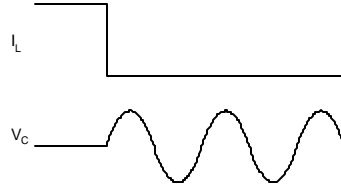
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Starting and Stopping on a Dime

- When circuit is *off*, inductor current is 0.
- During startup, the capacitor must supply current to the load while the inductor current ramps up
- Similarly, when the circuit shuts down, the capacitor must absorb the inductor current while it ramps down
- In either case, the situation is that of a step current into an LC circuit
- Response is a sine-wave



$$\Delta V = \frac{I_{\text{avg}}}{C_B \omega_C} \sin(\omega_C t)$$

$$= I_{\text{avg}} \sqrt{\frac{L}{C}} \sin(\omega_C t)$$

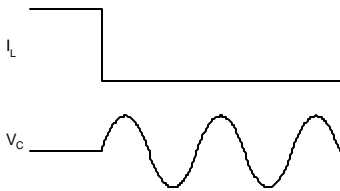
$$\Delta V_{\text{max}} = I_{\text{avg}} \sqrt{\frac{L}{C}}$$

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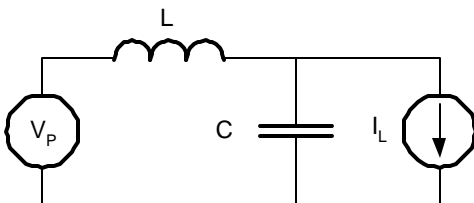
Bypass Capacitor to Handle Start/Stop Transient



$$\Delta V_{\text{max}} = I_{\text{avg}} \sqrt{\frac{L}{C_B}}$$

$$C_B > \left(\frac{I_{\text{avg}}}{\Delta V_{\text{peak}}} \right)^2 L$$

$$L_{i+1} < C_i \left(\frac{\Delta V_{\text{peak}}}{I_{\text{avg}}} \right)^2$$



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Sizing Bypass Capacitors

- Bypass capacitor must be sized to handle both types of inductive power supply noise
 - ripple due to non-uniform current within a clock cycle
 - start/stop transients
 - maximum ripple can happen at peak or trough of transient
- Approximate capacitance requirement by summing the independent requirements
- Usually several *stages* are required to meet both constraints

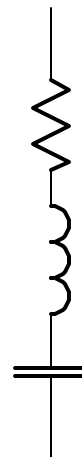
$$\Delta V_{\max} = I_{\text{avg}} \sqrt{\frac{L}{C_B}} + \frac{k_i I_{\text{avg}} t_{ck}}{C_B}$$

$$C_B > \left(\frac{I_{\text{avg}}}{\Delta V_{\max}} \right)^2 L + \frac{k_i I_{\text{avg}} t_{ck}}{\Delta V_{\max}}$$

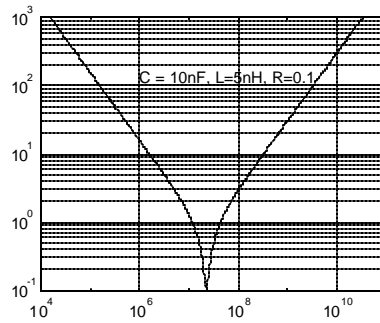
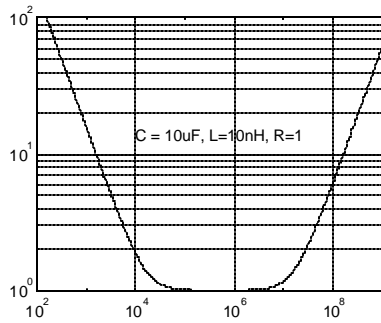
$$C_B > \left(\frac{I_{\text{avg}}}{\Delta V_{\max}} \right) \left(k_i t_{ck} + \left(\frac{I_{\text{avg}}}{\Delta V_{\max}} \right) L \right)$$

The Truth about Bypass Capacitors

- Most capacitors are only capacitors at low frequencies
- Capacitors have parasitic series resistance and inductance
- Every pico-Farad has its very own nano-Henry
- Two key breakpoints
 - LC frequency
 - RC frequency
- Capacitors are ineffective at bypassing currents above *either* of these frequencies



Impedance vs. Frequency for some Typical Capacitors



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Capacitor Properties

Type	C	R	L	f_{RC}	f_{LC}	f_{LR}
On-chip MOS	250fF	10	0	64GHz		
On-chip MOS	1pF	40	0	4GHz		
SMT ceramic	1pF	0.1	1nH		160MHz	
SMT ceramic	1nF	0.1	1nH		50MHz	
Ceramic disk	10nF	0.1	5nH		23MHz	
Al Electrolytic	10 μ F	1	10nH	160KHz		16MHz
Al Electrolytic	1mF	0.05	10nH	3KHz		800KHz


- High frequency is only achieved with small capacitors
- Many capacitors can be used in parallel to increase capacitance without reducing frequency

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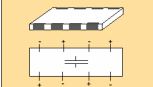
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Special Low L Capacitors Do Substantially Better

Low Inductance Chip Capacitors 

Interdigitated Capacitor (IDC)



GENERAL DESCRIPTION
 An interdigitated capacitor is a very low inductance, surface mount capacitor. A measured inductance of 175pH means that the capacitor's inductance does not contribute to the total inductance of the power distribution network. It is used for high speed microprocessors, digital logic, and beyond, the need for low inductance, decoupling capacitors between chips. In connecting the device with high speed to the power and ground planes, the inductance of the interdigitated capacitor can be ignored. This device is designed to handle the current, and the generation of microprocessors.

HOW TO ORDER

W L Y C 105 M A T 3 A

Size Code Inductance of Cap. Material of Cap. Voltage Rating Capacitance Code Inductance Multiplier Temperature Coefficient Code Package Code Lead Type EnduroLead Type

Package Style	Measured Inductance (pH)
105	175
105A	175
105B	175

Capacitance (pF)	047	0.1	0.22	0.47	1.0	2.2
X7R						
X7S						
X7T						

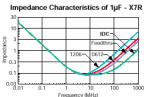
PERFORMANCE CHARACTERISTICS

Capacitance Tolerance	X7R
	+8%

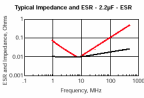
Dielectric Factor	X7R
	For 0.1 micro, 2.0 to 2.5 max. For 10 micro, 2.0 to 2.5 max. For 0.22 micro, 2.0 to 2.5 max.


Insulation Resistance (ESR@VDC)	X7R
	100,000kV min. or 1000kV min. depending on size.

Impedance Characteristics of 105 - X7R



Typical Impedance and ESR - 2.2pF - X7R





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Bypass Network Design Procedure

1. Start at the load and work out
2. At each stage, i
 1. Size the capacitance to handle the HF current $C_i > i_{it}/\Delta V$
 2. Size the capacitor as big as possible (economically) while keeping the inductance L_i small enough for the transient limit of the previous stage ($i-1$)
 - $L_i < (\Delta V/I)^2 \times C_{i-1}$
3. Done when capacitance is greater than $L_s(I/\Delta V)^2$

Really picking capacitors based on their inductance

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Example Design

- One chip, 10A, $t_{ck} = 2\text{ns}$, $k = 0.5$, $\Delta V = 0.1\text{V}$, $di/dt = 40\text{A}/0.5\text{ns} = 80\text{GA/s}$, $L_s = 100\text{nH}$
- First rank
 - $C1 > (0.5 \times 10 \times 2\text{n})/0.1 = 100\text{nF}$
 - $L1 < \Delta V/di/dt = 0.1/80\text{G} = 1.25\text{pH}$
 - Choose on-chip 250nF capacitor
 - Could get by with 100nF, but 250nF makes the next level easier
- Second Rank
 - $L2 < C1(\Delta V/I)^2 = 250\text{n}(0.1/10)^2 = 0.025\text{nH}$
 - First rank increases inductance limit by 20x (would have been 8x with 100nF)
 - Choose 10 2.2 μF IDC caps (175pH each) on package
 - And lots (100s) of solder balls to keep total L less than 25pH

Example Design (cont)

- Third Rank
 - $L3 < C2(\Delta V/I)^2 = 22\mu (0.1/10)^2 = 2.2\text{nH}$
 - Choose 5 1000 μF Ultra low ESR Tantalum capacitors
 - ESR of 0.018 Ω each, 0.0036 Ω total.
 - Current rating of 2.1A – 10.5A total
 - .036V ripple with 10A current
 - We're done since $C3 = 5000\mu\text{F} > L_s(I/\Delta V)^2 = 100\text{n} \times (10/.1)^2 = 1000\mu\text{F}$

A Typical Tantalum

TANTALUM CHIP CAPACITORS
T494 SERIES — Low ESR, Industrial Grade

KEMET

FEATURES

- Low ESR values in EIA 588AC sizes
- Taped and Reeled per EIA 481-1
- Symmetrical, Constant Terminations
- Optional Gold-plated Terminations
- Lead-free/roHS Compliant
- 100% Surge Current test on C, D, U, V, X sizes
- Capacitance: 0.1 μ F to 470 μ F
- Tolerance: $\pm 10\%$, $\pm 20\%$
- Voltage: 4-50 VDC
- Extended Range Values
- Thin Low Profile Case Sizes

CAPACITOR OUTLINE DRAWING

STANDARD T494 DIMENSIONS
Millimeters (Inches)

Case Size	L	W	H	Terminal Spacing	Terminal Diameter	Terminal Length	Terminal Width	Terminal Thickness	Terminal Spacing	Terminal Diameter	Terminal Length	Terminal Width	Terminal Thickness
S	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
T	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
U	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
V	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
X	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025

LOW PROFILE T494 DIMENSIONS
Millimeters (Inches)

Case Size	L	W	H	Terminal Spacing	Terminal Diameter	Terminal Length	Terminal Width	Terminal Thickness	Terminal Spacing	Terminal Diameter	Terminal Length	Terminal Width	Terminal Thickness
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T	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
U	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
V	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
X	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025

T494 ORDERING INFORMATION

Tantalum — Lead Material
Series — Standard Value — Code
T494 — Low ESR, Industrial Grade — Value Range
Case Size — A — Not Applicable
Capacitance Preferred Code — Capacitance Tolerance
Voltage Preferred Code — Voltage Tolerance
Part number example: T494M000000A5 (10 digits — no spaces)
KEMET Electronics Corporation, P.O. Box 5028, Greenville, S.C. 29606, (864) 963-8200

TANTALUM CHIP CAPACITORS
T510 SERIES — Ultra Low ESR

KEMET

FEATURES

- Ultra Low ESR < 20 m Ω
- Reel (J7780) Case with ESR < 10 m Ω
- Up to 4 Amps ripple current
- 100% accelerated electrolyte aging
- 100% Surge current test
- Precision matched, laser-matched cases
- Symmetrical constant terminations
- Taped and Reeled per EIA 481-1

OUTLINE DRAWING

DIMENSIONS - Millimeters (Inches)

Case Size	L	W	H	Terminal Spacing	Terminal Diameter	Terminal Length	Terminal Width	Terminal Thickness	Terminal Spacing	Terminal Diameter	Terminal Length	Terminal Width	Terminal Thickness
S	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
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U	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
V	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025
X	1.27	0.635	0.254	0.508	0.127	0.508	0.127	0.025	0.508	0.127	0.508	0.127	0.025

T510 RATINGS & PART NUMBER REFERENCE

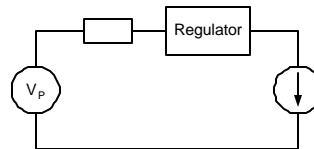
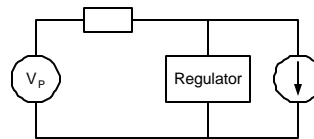
Cap. Code	Cap. Value	Cap. Tolerance	Voltage	ESR	ESR Tolerance	ESR Test Method	ESR Test Frequency	ESR Test Voltage	ESR Test Current	ESR Test Temperature
S	0.1	$\pm 10\%$	50	0.02	$\pm 10\%$	100	100	10	10	25
T	0.1	$\pm 10\%$	50	0.02	$\pm 10\%$	100	100	10	10	25
U	0.1	$\pm 10\%$	50	0.02	$\pm 10\%$	100	100	10	10	25
V	0.1	$\pm 10\%$	50	0.02	$\pm 10\%$	100	100	10	10	25
X	0.1	$\pm 10\%$	50	0.02	$\pm 10\%$	100	100	10	10	25

T510 ORDERING INFORMATION

Tantalum — Lead Material
Series — Standard Value — Code
T510 — Ultra Low ESR — Value Range
Case Size — A — Not Applicable
Capacitance Preferred Code — Capacitance Tolerance
Voltage Preferred Code — Voltage Tolerance
Part number example: T510M000000A5 (10 digits — no spaces)
KEMET Electronics Corporation, P.O. Box 5028, Greenville, S.C. 29606, (864) 963-8200

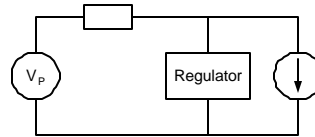
Local Power Supply Regulation

- Can put a regulator in series or parallel with the power supply
- Parallel or *shunt* regulators control current
 - add a current to the AC load current to make it look more like a DC current
- Series regulators control voltage
 - clip off the top of the voltage ripple and transient response
 - distribute power at a higher voltage (or AC voltage)



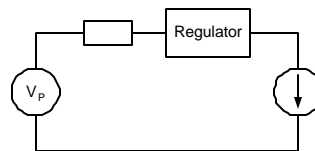
Shunt Regulators and Clamps

- Shunt regulators maintain a steady current draw from the distribution network
 - Measure the load current, I_L
 - Generate a shunt current
 - $I_R = I_{max} - I_L$
 - Current is now DC
 - but large
- A clamp handles the turn-off transient to avoid overvoltage
 - measure the load voltage, V_C
 - draw current when V_C exceeds a threshold



Series Linear Regulators

- Think of the regulator as a variable series resistor
 - drop distribution voltage (e.g., 3.3V) down to a load voltage (e.g., 2.5V)
- Can *clip* off the top of the voltage ripple by resistively dropping it
- Limited by
 - frequency response of the regulator (can't track fast transients)
 - series nature of regulator, can't divert transient inductor current



Switching Regulators

- A *switching* regulator uses a reactive element (usually a transformer or inductor) to convert the supply from one voltage to another with only a small loss in power
- Distributing power at a high voltage improves things quadratically
 - less current to distribute
 - more voltage to tolerate ripple
- Often advantageous to make this distribution voltage AC (at 0.1kHz to 1MHz)

$$V_D = kV_P$$

$$I_D = \frac{I_P}{k}$$

$$\frac{\Delta V_D}{V_D} = \frac{Z_D I_D}{V_D}$$

$$= \frac{Z_D I_P}{k^2 V_P}$$

Next Time

- On-Chip Power Distribution