
EE273 Lecture 7

Signaling Part Two

February 2, 2004

Heinz Blennemann
Stanford University
heinzb@stanford.edu

Today's Assignment

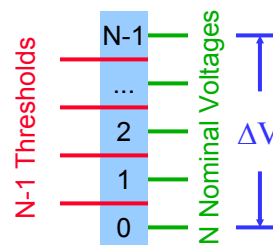
- Reading
 - Sections 8.1 through 8.4
 - Complete before class on Wednesday 2/4
- Midterm
 - evening of 2/11
 - 7PM to 9PM
 - local SITN students must come to Stanford for the exam
 - we will have class on 2/11

A Quick Overview

- Number of signal levels
 - binary vs multi-level signaling
- Some real driver circuits
 - bipolar current-steering driver
 - source-terminated voltage-mode driver
- Signaling over capacitive media
 - isolating power supply noise
 - current-mode signaling
 - references
 - pulsed signaling
 - SRAM example

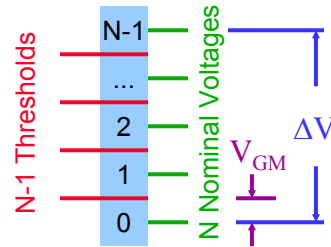
Number of Signal Levels

- There is nothing magical about 2-level or *binary* signaling
 - But its *almost* always the best choice
- Could use N-levels
 - N symbols
 - N nominal symbol voltages
 - N-1 thresholds
 - Nominal voltage separated from threshold by $\Delta V/2(N-1)$



Multi-Level Signals and Noise

- In the worst case, signal can swing through ΔV , from 0 to N-1
 - proportional noise is proportional to full swing
- Gross margin is distance from nominal voltage to threshold
- Proportional noise constant, K_N must be kept very small to allow more signaling levels
- Number of bits per symbol is $\log_2(N)$



$$V_{GM} = \frac{\Delta V}{2(N-1)}$$

$$K_N = \frac{1}{2(N-1)}$$

Multi-Level Signals and Power

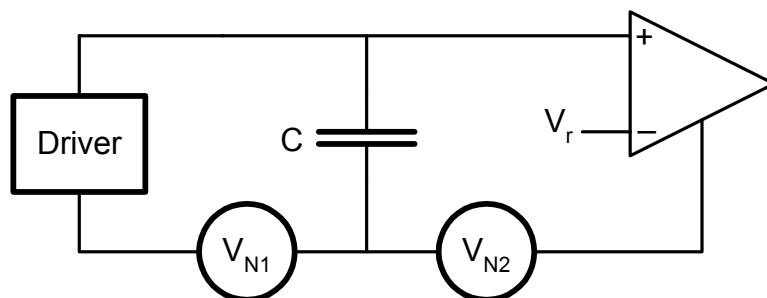
- Power per symbol (worst case) is proportional to ΔV^2
- With fixed noise sources this grows as N^2 .
- So power per bit grows as

$$\frac{N^2}{\log_2 N}$$
- So why use multilevel signaling?
 - when channel is band-limited
 - it may be the *only* way to get more bits over a channel
 - AND when there is a very large SNR
 - so proportional noise doesn't swamp the multi-level signal.

Signaling Over Capacitive Media

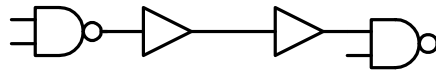
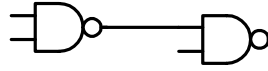
- Where do we find capacitive wires?
 - short on-chip wires with high fan-out or fan-in
 - e.g. buses, register files, RAMs
 - note that long on-chip wires are RC lines - a more difficult problem
- Desiderata
 - fast transitions
 - low power
- These imply a small signal swing
 - to support a small swing one needs to isolate power supply noise

Block Diagram of Capacitive Signaling System



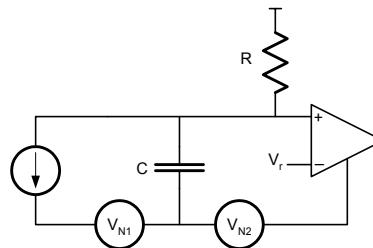
Logic Signaling vs Transmission Signaling

- Historically signal levels were defined to facilitate *logic circuits* not *transmission*
 - for example:
 - 0 = TGND, 1=TVDD
 - $V_f = (RGND + RVDD)/2$
 - slow
 - lots of power dissipation
 - no rejection of supply noise
- When transmission is a large fraction of delay or power, its better to switch to a representation tailored for transmission

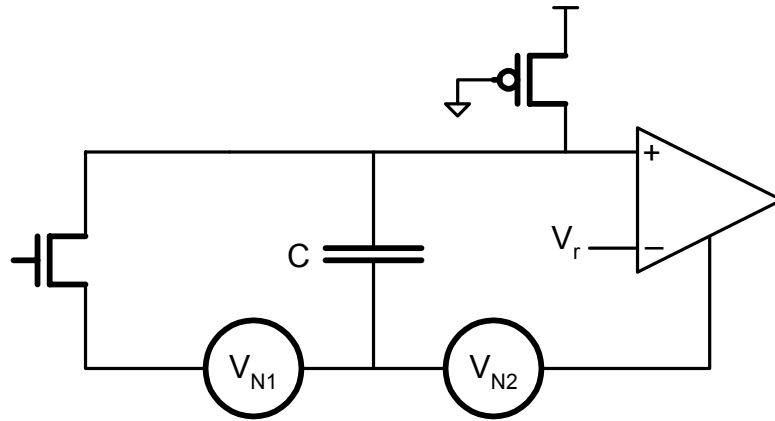


Current-Mode Signaling

- Send logic values as small currents
 - 1=1mA
 - 0=0mA
- Detect across 'resistor' at receiver
- High Tx impedance isolates Tx supply noise
- High-pass RC removes low-frequency Rx supply noise
- Still need to generate a reference

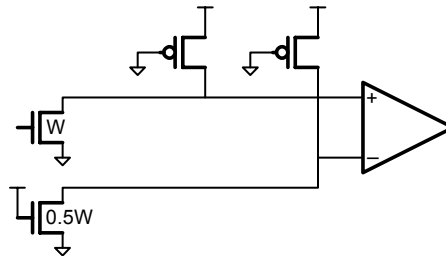


A Current-Mode Signaling Circuit



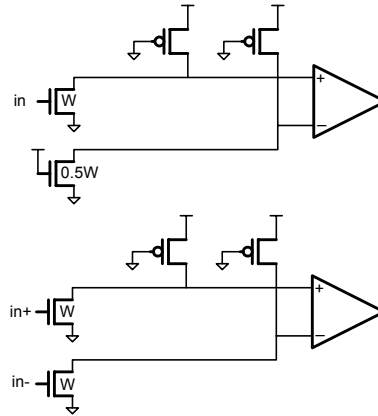
Transmitter References

- Would like to set receiver reference half-way between a '1' and a '0'
- Simplest approach is to send half the '1' current from the transmitter
 - this reference can be shared by many signals
- If drive current is 1mA, signal swing is 0.3V, and capacitance is 3pF, what is the rise time?
 - how does it depend on signal swing?



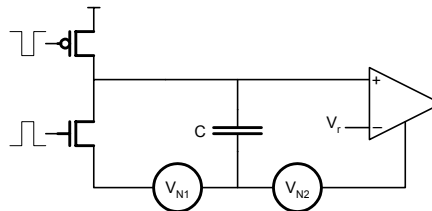
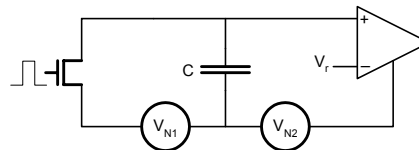
Differential Signaling

- If wire tracks are available, best noise cancellation is to send the signal and its complement
 - *twist* the signals periodically to balance crosstalk
 - better noise rejection
 - balanced load on the two lines
 - twice the signal swing for the same current (or half the rise time)
- But this still dissipates DC power!



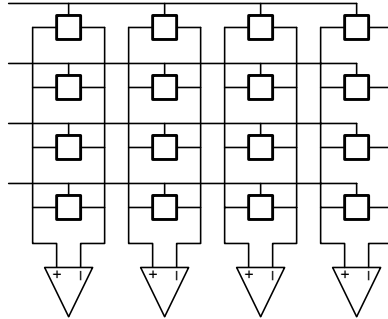
Pulsed Signaling

- To eliminate DC power dissipation just
 - (1) remove the 'resistors'
 - (2) drive the line with current *pulses*
- What does (1) do to noise rejection?
- How do we set the DC level of the line?
 - precharge
 - feedback
 - self-timed pull-down
- Do we need to pulse the line in both directions?



Case Study, SRAM Bit Lines

- SRAMs have high fan-out on the word lines and high fan-in on the bit lines
- Bit lines use differential, pulsed, precharged current-mode signaling
- Typically have 50mV to 300mV swing
 - careful ground rules to make all crosstalk common mode
- Detected with clocked amplifier 30mV offset+sensitivity



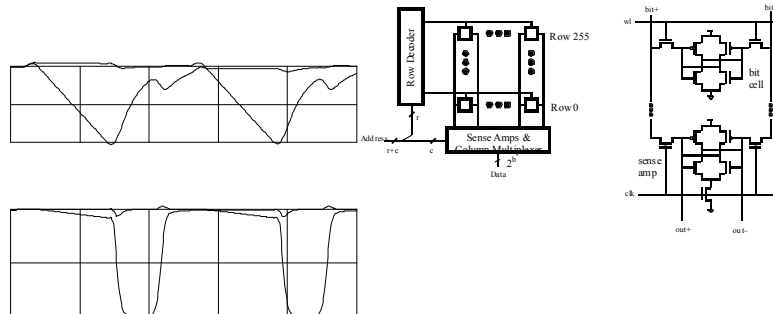
SRAM Numbers

- Typical *subarray*
 - 256 rows x 1024 columns
 - 0.5pF bit line, 2pF word line
 - on-current is 0.2mA
 - pulse width is 500ps

$$\Delta V = \frac{It}{C} = \frac{(0.2\text{mA})(0.5\text{ns})}{(0.5\text{pF})} = 200\text{mV}$$

- How long would it take to go full-swing (1.8V) ?

SRAM Waveforms



Next Time

- Signaling wrapup
- Dealing with long on-chip RC lines
- Dealing with lossy LRC lines
- Simultaneous bidirectional signaling