

CSE464 Homework 11 Due 2005.05.02 4PM

Note: Please list at top of first sheet of homework submission anyone or anything from which you obtained any help for this homework assignment other than the text, class notes/discussion, and the instructor. Please give a word or two as to the nature of the help (e.g.: discussed problems, copied verbatim, whatever). Acknowledging source of help is a requirement for this assignment, and for all assignments in CoE464. It has no effect on your grade (unless you forget to do it).

Problem 9-2 from the text.

1. Slides 19 and 21 of Dally-Blennemann Lecture notes 12 on closed loop timing show bundled and per-line closed loop timing. Given the following component parameters, what is the maximum data transmission rate for each? Skew between components is +/- 10% of delay except for transmission line which is 1% of delay. Jitter is +/- 10% of delay except for transmission line which is zero.

0.4 ns	flip-flop t_{dcq}
0.1 ns	t_a
0.1 ns	rise/fall time of signals
0.3 ns	input or output buffers
6 ns	transmission line
0.1 ns	max error in phase comparator and clock feedback circuit
0.1 ns	max error in $\pi/2$ delay
0.1 ns	peak-to-peak jitter in the clock (ϕ_{tx} and ϕ_{rcv})
0.05 ns	offset of center of aperture time between two flip-flops

2. The Xilinx BG492 FPGA package has the following parameters:

value	parameter	units	conditions
17.2	Theta _{ja}	C/W	still air
12.2	Theta _{ja}	C/W	250 feet/min air velocity
11.9	Theta _{ja}	C/W	750 feet/min air velocity
0.8	Theta _{jc}	C/W	

If a heatsink is used, θ_{c-hs} is 0.2 C/W. With max allowed junction temperature of 100 C, and ambient temperature of 50 C:

- A) what is max power dissipation without heatsink in still air
 - B) what is max power dissipation without heatsink with 250 feet/min air velocity
 - C) Using Wakefield heatsinks (<http://www.wakefield.com/pdf/BGA.pdf>) type 655-26AB and 655-53AB, what air velocity is needed for power dissipation of 16 W?
3. A pair of coupled transmission lines have $R_1=50$ Ohms and $R_2=400$ Ohms. The near end of line 1 is driven by a series terminated driver ($R_s=50$ Ohms) and the far end of line 1 is open circuit. The far end of R_2 is driven by a series terminated driver ($R_s=50$ Ohms) and the near end is open circuit. Both odd and even mode propagate with the same velocity. The near end driver switches from 0V to 1V at $t=0$. What is the voltage at the driving end of line 2 when the first transition arrives?
 4. <http://www.embedded.com/showArticle.jhtml?articleID=55801076>
http://www.xilinx.com/products/virtex4/pdfs/BGA_Crosstalk.pdf

The first link above is to an article relating to signal-return crosstalk problems with FPGA and other packages. The second link is to a paper describing measurements on two FPGAs. Comment on the methodology used for the measurements, and on the results.