

CSE464 Homework 10 Due 2005.04.20

Note: Please list at top of first sheet of homework submission anyone or anything from which you obtained any help for this homework assignment other than the text, class notes/discussion, and the instructor. Please give a word or two as to the nature of the help (e.g.: discussed problems, copied verbatim, whatever). Acknowledging source of help is a requirement for this assignment, and for all assignments in CoE464. It has no effect on your grade (unless you forget to do it).

1. Read the article: "Ground Bounce" by Bob Colwell in the March 2003 edition of IEEE Micro, pp 11-13. It is available at: <http://www.computer.org/computer/homepage/0303/random/> (earlier version of this had access via Olin, this seems to work better). There is a limit to the number of subscribers that can simultaneously access the IEEE publications so if everyone tries to do it at 3:30 on the day the assignment is due, some will not get access. A similar problem to the one described in the article occurred with a custom IC developed for interconnection of processors in a hypercube pattern, one of the early configurations used for parallel processing. The network was designed for byte-wide transfers (8 bits in parallel) but failed due to ground bounce. Fortunately for the developers, they were able to change the operation to nibble-wide (4 bits) and use the original custom ICs, although at half the intended data rate. Problems due to ground bounce (signal return crosstalk) are probably more common than we realize. There are probably many systems in operation now that have occasional errors because of ground bounce, but because they are so infrequent the cause is not identified. Perhaps you own something with this problem?

Many designs are based on the expectation that if something worked last time, it will work next time. Frequently ignored are changes in parameters or context that make this expectation wrong. Shorter rise and fall times are perhaps the most common change invalidating new designs, but there are many more.

Pay particular attention to the last column. Component manufacturers are not always as helpful as they might be. Some times it even seems that they are adversaries. They are not really working against you, it just seems so sometimes as they try very hard to avoid giving you any "bad news".

The problem described by Colwell also appeared in an article on front page of the July 26, 1986 edition of *Electronic News*. ACL (advanced CMOS logic) circuits by TI and Signetics encountered the same problem. Eventually they went to placing Vdd and ground on the center pin of each side of DIP packages to reduce inductance and ground bounce (signal return crosstalk). As Colwell says, the small-outline packages have much shorter leads and thus lower inductance, the question is whether the same mistake will be made again and again (answer: yes). As rise/fall times continue to decrease, the packages that worked last time may not work next time. You might consider how we keep from repeating mistakes of the past. Even some of us who should know better have repeated past mistakes with well known and undesired consequences.

2. Study the phase-slip detector and xp/rp generation circuit in Figure 10-17 of the text. Is it correct? Why are there two sets of flip-flops in series between t_m and sdxp? Would you recommend any changes? This is plesiochronous timing.
3. Design (logic schematic) a circuit to transmit data between two independent clock domains where you have no knowledge about the two clocks except that their average frequencies are

within a two to one ratio over any 5-clock period (during 5 clock periods of one domain, there will not be more than 10 clock periods in the other). Performance is not an issue but don't take extra effort to reduce performance. Within each clock domain it is not necessary to carry out detailed design, you may merely provide and receive appropriate signals (in the local clock domain) to/from other (undefined) logic.

4. Study and understand operation of the circuit in Figure 2 of <http://www.edn.com/article/CA152876.html> (and passed out in class). Do you identify any possible problems with this circuit?

CSE564: Look at a flip-flop with respect to metastability (be prepared to discuss this next Monday). How does a flip-flop differ from a latch (if it does) with respect to metastability?