

CSE464 Homework 09 Due 2005.04.13

Note: Please list at top of first sheet of homework submission anyone or anything from which you obtained any help for this homework assignment other than the text, class notes/discussion, and the instructor. Please give a word or two as to the nature of the help (e.g.: discussed problems, copied verbatim, whatever). Acknowledging source of help is a requirement for this assignment, and for all assignments in CoE464. It has no effect on your grade (unless you forget to do it).

1. Following on to problem 3 from HW#7, consider using one of these FPGAs as a clock buffer. Data on the DLL characteristics are given on page 13 of the data sheet. No information that I could find is given on the matching of delay between outputs from the FPGA so we will *guess (not the best procedure, if you have a way to get better data use it)*. Take the mismatch in delay between outputs to be +/- 10% of the total delay (10% of 4.7ns for delay without DLL, or 470 ps), and calculate the characteristics (skew, jitter, ...?) of one of these FPGAs used as a clock buffer. Xilinx App Note 132 (<http://www.xilinx.com/bvdocs/appnotes/xapp132.pdf>) gives an example of this in Figure 10. Multiple OBUF elements could be used to drive multiple clock lines in parallel.

Just for fun: look at the various I/O levels given on pages 3 and 4. You might ask if all of these are necessary (or useful). Of course there are others, they are just not available on this part. Note that some I/O standards use Vdd (Vcco) of 2.5V, some use 3.3V, some use 1.8V.

2. A high-speed communication system with a 200Mhz clock and many asynchronous inputs exhibits occasional failures. An experiment is performed in which the system is run continuously for 24 hours with clock period of 4.8ns, then 24 hours with clock period of 5ns, then 24 hours with clock period of 5.2ns. The number of failures for the 24 hour periods are 27, 5, and 1 respectively. Does this prove that metastability is the cause of the failures? Assuming metastability is the cause of the failures, estimate the value of τ_s (resolving time constant) for flip-flops in this system if all flip-flops are identical. To simplify the calculation, you may take the clock frequency, but not the waiting time, as approximately constant (a few hundred ps difference in clock frequency makes very small difference in calculated probability of failure). If the allowed failure rate is to be less than one failure per 100 years, what clock period would be required? Since increasing the clock period may not be acceptable, suggest design changes other than increasing the clock period that might be used to obtain an acceptable failure rate.
3. A redesign of the synchronizing flip-flop in the circuit of problem 2 is possible to reduce its value of τ_s by 20%. Can you determine how much this would improve operation with the original clock parameters? If you need additional parameters or data, make your best guess at to appropriate values.
4. The schematic shows part of the clock and data path for an HDLC (HDLC is the protocol) bus using RS-485 signaling. This is a differential serial bus with separate clock and serial data. RS-485 is a *slow* differential signaling protocol. Important delay values are given in the schematic. The actual system contains 32 PC cards which partially explains why the data delay can be so long. The schematic shows only a few connections but is adequate to analyze worst case timing. You are to analyze the timing, identify any flaws, and suggest corrections.

The 1480 transceiver by Linear Technology is particularly slow (URL for data sheet although you don't need it for this problem: go to <http://www.linear.com>, and search for LTC1480. You should find a one page summary, and link to a complete data sheet). A faster pin and

electrically compatible device is available from Maxim and this was originally specified for this application. Somehow, the Linear Technology part was substituted without significant review as to the differences (after all, *the clock frequency is only 1 MHz*). Many systems have been assembled using the 1480 transceiver and all have functioned flawlessly (after usual debugging) through extensive testing including temperature extremes, max and min Vdd, and many others. The Maxim part has shorter propagation delays but is fabricated in CMOS instead of bi-polar, and turns on at a slightly lower Vdd voltage. Your co-workers are afraid to substitute the faster Maxim parts because of system reliability issues. If a card loses power, its 3.3V Vdd (from which the 1480 transceivers are powered) may still be 1.5 V or so because some power is supplied through IC protection diodes from powered signals connected to other PC boards. If the transceiver turns on and loads this HDLC bus, it could cause bus failure. There are two HDLC busses for redundancy but the same problem could cause both to fail, thereby causing the system to fail since this bus is critical to low-speed status transfers that are required for system operation. Note that during the original design it might have been possible to set the clock to a lower frequency. A lower frequency is no longer possible because there are many programs that *may* depend on the bus operating at its 1 MHz clock rate. It is possible that a lower frequency would work, but there is so much software, and so many conditions that would have to be tested that everyone (especially those who count) absolutely refuse to consider this fix. Once a system has been (largely) debugged and is operating, changes need to be considered very very carefully. It's too easy to break one thing (or things) while fixing something else, way too easy. The clock for this circuit is generated from a much higher frequency by a PLD (programmable logic device so there is considerable freedom in the waveform and duty cycle, even if the frequency must be kept unchanged.

5. The circuit shown on the schematic is suggested for terminating the data signal for the HDLC bus. It provides 120 Ohm differential termination at each end of the data line. The data lines are designed to each have 60 Ohm characteristic impedance to ground, and essentially no coupling between them, giving differential impedance of 120 Ohms. The bus is driven by up to 32 transceivers, each with its data signal tied HIGH, only one transceiver is enabled at a time. If none are enabled the data bus value is L since the resistors pull DP (data positive) line low, DN (data negative) line high. A driver drives an H level on the line by pulling the DP line high and the DN line low, when the driver is enabled. When no transceiver is enabled, the differential voltage is 3.3V, much larger than the 200 mV required by the receivers. A difference voltage of 1 V is more than adequate, even with noise, reflections, etc. Look at the specification sheet for the transceivers (go to: <http://www.linear.com>, and search for LTC1480. You should find a one page summary, and link to a complete data sheet) and evaluate this design. Is it ok? Do you have suggestions for an alternative? The parameter of most interest for this problem is: Differential Output Voltage, V_{OD2} and you should look at the output current specification vs. the current required by the given termination. Note that the plot of "Driver Differential Output Voltage vs. Output Current" is for typical conditions, not worst case. Worst case is given in the table of Electrical Characteristics. We like our designs to work for worst case, not just typical, conditions.

CSE564 ONLY: Reducing the separation between power and ground planes increases the capacitance and reduces the inductance, both are good for power supply distribution. It is also possible to increase capacitance by using an insulating material with a higher dielectric constant (this is commercially available). Does increased capacitance from higher dielectric constant provide an advantage? Opinions differ dramatically on this as some insist it is now necessary, others say it does not help. Consider various cases: A) Uniform transmission line with open circuit at far end; B) uniform transmission line with short circuit (AC) at far end; C) radial

transmission line (from vias out across PC board) with open circuit at some radius; and D) radial transmission line with short circuit at some radius. Note that one can consider the L and C of the planes, or they can be considered as a transmission line with some (possibly non-uniform) Z_0 .