

EE464 Homework 08 Due 2005.04.06

Note: Please list at top of first sheet of homework submission anyone or anything from which you obtained any help for this homework assignment other than the text, class notes/discussion, and the instructor. Please give a word or two as to the nature of the help (e.g.: discussed problems, copied verbatim, whatever). Acknowledging source of help is a requirement for this assignment, and for all assignments in CoE464. It has no effect on your grade.

1. Read: "Why Johnny Can't Design a High-Speed Digital System",
http://www.conted.ox.ac.uk/cpd/electronics/links/why_johnny_cant_design.asp Any "big picture" comments on this? Disagreement allowed!
2. Problem 9-5 from the text.
3. If two MPC961 clock drivers are used in parallel to drive multiple clock signals from a single oscillator, what is worst case skew and jitter at the clock receivers? All interconnections are series terminated transmission lines with length tolerance of +/- 0.1 inch, propagation velocity of 2ns/ft, and inputs have capacitance tolerance of +/- 2 pF. Note that with a circuit such as this, its possible to generate an "early clock" by making the feedback connection longer than the clock distribution connections.
http://e-www.motorola.com/files/timing_interconnect_access/doc/data_sheet/MPC961C.pdf
4. In Lee Ritchey's note: "How poor packaging kills good PCB designs", he gives an example of a PC board with 140 nF of power supply bypass capacitance due to the power and ground plane parallel plate capacitance. If there is a single power and single ground plane with 4 mil separation and ϵ_{r} of 4, how large a PC board is required to obtain 140 nF of capacitance? If the PC board is to be 8" by 8", how many power-ground layers would be required to obtain 140 nF of capacitance. Not necessary for this problem, but if you are interested the note can be found at the link given on the HW assignment page.
<http://www.eedesign.com/features/exclusive/showArticle.jhtml?articleId=17600827&kc=4235>
5. Hyperlynx is a program to aid in the design of digital systems by analyzing and simulating signal propagation. It is available on the CEC systems, including on oasis via remote desktop. Hyperlynx tutorial is under Hyperlynx 7.2 in the engineering folder. Run the tutorial and give a brief evaluation of the program. Since this is an open ended problem on which you could easily spend days, limit yourself to no more than 2 hours for this problem. You may choose to explore one part in detail, or look more globally at the program. For the part you explore, please indicate what you understand, don't understand, believe could be done better, and what you particularly like or believe is well done. Note that this program lets you import schematics and carry out SPICE or other electrical simulations, no text-based SPICE file need be generated. It also serves as a "virtual prototyper" letting you explore options before complete design is finished. One page of evaluation is adequate for this problem, no need to write a complete and extensive report. One part you may wish to evaluate is eye-diagram generation under you through use and evaluation of the program. Note: when I tried the eye-diagram tutorial the models used were not the ones mentioned in the tutorial but they seemed to work fine.

A few years ago I had a Xilinx publication (I believe) describing two quick-and-dirty workarounds for clocking problems caused by inadequate attention to digital systems engineering issues. I cannot find it now. If any one can help me find a copy I could generate a couple of interesting HW problems from it.

CSE564 Only: Read and understand “Short-Term Impedance of Planes” by Howard Johnson in his online newsletter at: <http://www.sigcon.com/> (Follow the link under “Archives”). Verify (or not) his conclusions for one-cm radius planes, using HSPICE simulation with a series of transmission line segments. Feel free to also verify for larger planes but if you do so, you may want to generate the HSPICE statements automatically, or find some clever way to use macros and/or parameters (I don’t know if this can be done or not). Typing a hundred or so transmission line statements is certainly possible but can become boring (and error prone). Feel free to include resistance for damping, but it should not be necessary for this problem. Major effect of resistance would be to reduce the amplitude of the resonance peaks. Hint: for avanwaves plots select log scale for y-axis under the graph menu. Linear scale obscures every bit of detail.

- A. Do you get similar results to those reported?
- B. Calculate the capacitance and inductance for this structure, and compare resonant frequency and LC circuit with these values to the simulation result.
- C. Calculate the round-trip delay from via to edge of the plane and compare to the resonant frequency. Do they correspond? Why or why not?
- D. What change would you expect with a more representative separation between planes for dense high-speed design, say 7.5 mils rather than 30 mils? 3 mil separation?
- E. What would you expect if there were a large number (e.g., 128) signals similar to the one being analyzed that pass through vias?