

CSE464 Homework 07 Due 2005.03.30

Note: Please list at top of first sheet of homework submission anyone or anything from which you obtained any help for this homework assignment other than the text, class notes/discussion, and the instructor.

Please give a word or two as to the nature of the help (e.g.: discussed problems, copied verbatim, whatever). Acknowledging source of help is a requirement for this assignment, and for all assignments in CoE464. It has no effect on your grade.

1. A PC board is 10" by 10" and has Vdd and GND 1-oz copper planes separated by 4 mils of FR4 dielectric with relative dielectric constant of 4. To simplify grading please arrange answers in a 4x3 table, with parameter (a through d) in rows, and board type in columns.
 - a) What is the plane to plane capacitance?
 - b) What is the inductance between two 20 mil vias in the center of the board, one connected to GND and one to Vdd, to the circumference of the board if the circumference is approximated by a circle with a radius of 5 inches?
 - c) What is the resistance (sum of both planes) from the 20 mil vias to the board circumference, approximated as above (5 inch radius circle)? 1 oz copper has resistance per square of 0.5 mOhm.
 - d) What is the propagation delay from the vias to a point 5 inches away
 - e) What are the new values for above parameters if the board is manufactured with 20 mil separation between the planes?
 - f) What are the new values for above parameters if the board is manufactured with a new process that gives plane to plane separation of 2 mils, and has a relative dielectric constant of 20?
2. 48V is supplied to a (large) piece of telecommunications equipment by two 100 foot bus bars (48V and 48V return), each 0.5 inch by 1 inch. They are separated on the 1 inch dimension by an insulator with relative dielectric constant of 4, and a thickness of 0.05 inch.
 - a) Calculate the characteristic impedance of this as a transmission line (use parallel plate approximation, ignore edge effects).
 - b) Calculate the voltage loss from DC resistance (copper conductors) with a 200A load.
 - c) If the source power supply is perfect (48V, 0 Ohms), the load is 200A connected by a circuit breaker located adjacent to the load, and the breaker opens in zero time, what is voltage on the 48V bus at the breaker just after the breaker opens?
 - d) If it is desired to keep the transient voltage (increase over DC value) to less than 20V, what impedance would be required for the bus?
 - e) To achieve the impedance calculated in d), what capacitance would have to be added to each foot of the 48V bus? This may not be a practical solution, but makes a good homework question.
3. EE462 uses Xilinx XC2S150-5 FPGAs in their designs. Consider the question of maximum clock rate that can be used if two of these ICs communicate with each other in a common clock domain. Assume the clocks for the two ICs are generated by a common clock buffer with (including oscillator that drives the buffer) skew between clock buffer outputs of +/-300ps, jitter of 100ps peak

(200ps peak-to-peak), clock distribution traces matched within 0.2 inches, and loads at the clock receivers of 4pF +/-2pF. Clock distribution transmission line impedance is 50 Ohms, propagation velocity is 1ft/2ns. What is minimum delay allowed from clock to output of one FPGA? What is maximum clock frequency allowed? Calculate these both for DLL, and no DLL. Use FPGA data for 12mA LVTTTL standard I/O. The XC2S150-6 data sheet is available at:

http://www.xilinx.com/bvdocs/publications/ds077_3.pdf

Use the delay values given on pages 5 and 6 of this data sheet.

4. Problem 9.4 from text. Note that two flip-flops in series with the clock to one of them inverted could also be used. This allows use of conventional flip-flops which may be more readily available (total of 4 latches, two for each flop), but is not as efficient as the given implementation which uses three latches. This scheme is used in some low speed applications (JTAG serial test bus and configuration load for FPGAs) where speed is not important, and where clock skew may be hard to control. Although requiring more flops than conventional clocking, the savings in design analysis and clock skew control can be a very good tradeoff in some low performance applications.
5. This problem deferred until I have a chance to evaluate the full Hyperlynx simulation program. It is now available to us. Download the Hyperlynx software demo at: <http://www.mentor.com/go/pcb7a> and evaluate it. The first page of text contains a link to a “front-to-back HyperLynx Simulation” which you can use to guide you through use and evaluation of the program. Since this is an open ended problem on which you could easily spend days, limit yourself to 2 hours for this problem. You may choose to explore one part in detail, or look more globally at the program. For the part you explore, please indicate what you understand, don’t understand, believe could be done better, and what you particularly like or believe is well done. Note that this program (at least the full version) does let you import schematics and carry out SPICE or other electrical simulations, no text-based SPICE file need be generated. It also serves as a “virtual prototyper” letting you explore options before complete design is finished. One page of evaluation is adequate for this problem, no need to write a complete and extensive report.

For review if you are uncomfortable with conventional clocking setup and hold time problems. Problem 4 from CoE260 homework assignment. It is suggested that you know how to solve these problems because a similar problem is highly likely on the next exam: <http://www.cse.wustl.edu/~dzar/class/260/hw/hw8.pdf>. Be sure to give the constraints on inputs (time that inputs must be valid with respect to the clock).

CSE564 Only:

Follow on to problem from Assignment 5 for the ambitious. Find the value of Z_0 (termination from each line to ground) that gives zero reverse crosstalk at receiving end when lines are terminated at both ends.

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Just for fun and understanding, not for grade:

Another transmission line simulator is available at:

<http://www.ece.concordia.ca/~trueman/bounce/index.htm>

Download the “bounce” program. A little harder to use, but more flexible than the previous one we used. This simulator allows control of rise time. Try simulating some poorly terminated (large reflection coefficient) cases first with short rise time, then with rise time several times the round trip delay. Note how the maximum values of undershoot and overshoot become much smaller as the ratio of rise time to round-trip delay increases. This is another reason (in addition to the signal-return crosstalk in HW5) that design becomes more difficult with faster circuits (unless we can also reduce line length proportionally, usually this is not an option). It is also a reason that “faster circuits” may some times be slower. Replacing an IC with a functionally equivalent one with smaller transition times may cause failure in a system that works fine with the slower circuit. For equations to predict amplitude with long transition times, see the paper by O. Anthony Horna, “Pulse Reflection in Transmission Lines”, IEEE Transactions on Computers, December, 1971, pp1558-1561. Equations are given for maximum amplitude based on reflection coefficients and ratio of rise time to line delay.