

CSE464 Homework #6 Due 2005.03.23

Problem 5-12 in Dally and Poulton has the following possible solution to maintain ΔV less than 165 mV. This solution was given in a solution set for a previous year.

Rank 1: $C=60$ nF on chip capacitance, R and L are approximately zero

Rank 2: 12 SMT (surface mount) capacitors with total $C=120$ nF, $R=0.0083$ Ohms, $L=83.3$ pH

Rank 3: 60 Electrolytic capacitors with total $C=600$ uF, $R=0.017$ Ohms, $L=166$ pH (the large number of capacitors was chosen to obtain low resistance)

3.3 V power supply with equivalent inductance of 1 uH

Carry out the spice transient simulation (using HSPICE). Also find the impedance vs frequency over the range from 1kHz to 1GHz using HSPICE simulation (use a current source to drive the impedance, voltage will be $Z*I$). If current source is 1A, 1mV will correspond to 1mOhm. Note that impedance magnitude vs frequency has peaks at approximately 100MHz and 6Khz.

Note that there are two separate simulations specified, a transient simulation and a frequency simulation. There are many variables available to examine and plot. For the AC simulation the Voltage magnitudes are of most interest.

The peak in voltage (and thus impedance) for frequency response at 100MHz should make you curious as to what would happen if the period for the I_{dd} transient were changed to 10ns, rather than 6ns, and a new transient simulation performed. Try it! Comments? Note that digital systems are sometimes operated below their design frequency for debugging or other reasons. Note also that bypass components will not be available with zero tolerance on their values. Finally, it would be possible to generate some energy at about the 6 KHz peak by operating the clock for repeating intervals of 83us on, and 83us off (the ambitious student might try this).

Turn in:

1. Plots of transient and frequency response.
2. *Your analysis and comments on the plots and what they show.* Please either type your comments, or write neatly and in equivalent of at least 12-point type.

[Link to a .sp file](#) that should make this assignment fairly straightforward (at least should save you effort on generating spice source). It is strongly recommended that you generate the circuit schematic from the .sp file in order to check for errors, and to improve your understanding of spice commands.

2. Page 82 of “Computer Circuits: Electrical Design” by Ron K. Poon Suggests RMS summing of AC noise sources. In an example he gives the following values for ECL logic:

DC Noise Sources	Logic H Level
Ohmic Drop	50 mV
Skin Effect	15 mV
Voltage Differential	10 mV

Temperature Differential	20 mV
TOTAL DC	95 mV
AC Noise Sources	
Reflection	110 mV
Crosstalk	90 mV
Simultaneous Switching (Signal Return Crosstalk)	80 mV
Power Supply Ripple	10 mV
EMI (Electromagnetic Interference)	30 mV
Gate I/O Level (???)	50 mV
RMS total AC	173 mV
DC + RMS total AC	268 mV
Device Margin (Vm)	270 mV

Ignoring for the moment that we don't know the exact definition and/or description for some of the noise sources (EMI, Gate I/O Level, ...), what do you think of the methodology used here? Note that the difference between calculated noise level and noise margin is only 2 mV.

3. Comment on the following paragraph from a book on high-speed digital system design:

“For short lines, when the minimum digital pulse width is long compared to the time delay (TD) of the transmission line, source termination is desirable since it eliminates the need to shunt a portion of the driver current to ground. For long lines, where the width of the digital pulse is smaller than the time delay (TD) of the line, load (receiving end) termination is preferable. In the latter case, there will be multiple signals traveling down the transmission line at any given time (this is know as pipeline mode). Since reflections off the load will reflect back toward the source and interfere with the signals propagating down the line, reflections must be eliminated at the load.”

CSE564 Only (this problem will be discussed on March 21): You are to recommend the stackup (sequence of PC board layers) for a new high-performance network switch using PC boards similar to the example I have shown several times in class. This system has several different PC board designs, the boards have many wide (64- or 128-bit busses), connectors to a backplane, and connectors to daughter boards, and (because of unfortunate arrangement of pin ordering on ICs) several places where vias must be used to move all signals from one signal layer to another in order to transpose the bit order. It has been decided that GND and Vdd planes will be used that extend over the entire PC board, and as many planes as necessary will be used. In order to reduce EMI, only components, no traces, will be placed on the outer layers. All traces will be 50 Ohm controlled impedance, and will be terminated at one end or the other (or both) if analysis indicates they should be. The ICs are CMOS with symmetric H and L impedance and symmetric transfer characteristics and noise margins. Only a single signal layer will be placed between planes (GND or Vdd planes) in order to avoid what the text calls perpendicular crosstalk. There are two Vdd voltages, 2.5V and 1.5V, approximately half

of the circuits use one, half the other. These will not be cheap PC boards! Two choices are available for the GND and Vdd plane assignments as illustrated below.

Layer	Proposal A	Proposal B
1	Surface, component mounting	Surface, component mounting
2	GND	GND
3	signal	signal
4	GND	Vdd2.5
5	signal	signal
6	GND	GND
7	signal	signal
8	GND	Vdd1.5
9	Vdd1.5	signal
10	GND	GND
11	Vdd2.5	signal
12	GND	Vdd2.5
13	signal	signal
14	GND	GND
15	signal	signal
16	GND	Vdd1.5
17	signal	signal
18	GND	GND
19	Surface, component mounting	Surface, component mounting

Proposal A has the Vdd planes sandwiched between GND planes while Proposal B distributes the Vdd planes. The plane to plane (or plane to signal) spacing is the same for all layers. Compare these two stickups and determine whether either is preferred, or under what conditions one is preferred. Criteria might include GND to Vdd capacitance/inductance for power supply bypassing, noise generated by signal return current, number of signal layers for a given board thickness, ... Do you have any recommendations or guidelines for routing rules (which signal layers to use for specific signals, bypass capacitor requirements, ...)?

Just for fun, nothing to turn in, will not be exam material:

If you ever have nothing to do, and wonder why systems sometimes fail, try the following link. Either the archives or the latest issue. Many problems have to do with programming, specification, and user-interface issues, but some have unknown causes, and some are clearly computer engineering related (e.g.: ferry computer-controlled steering turns hard right when cell-phone is used).

<http://catless.ncl.ac.uk/Risks/>

Long running discussion on si-list about odd and even modes on transmission lines (search for odd and even modes). Shows that many engineers presently

working on digital systems engineering issues have a poorer understanding of this than you do, regardless of how poor your understanding is. And of course, some have excellent understanding.

<http://www.freelists.org/archives/si-list>