CSE464 Homework #3 Due 2005.02.16

Note: Please list at top of first sheet of homework submission anyone or anything from which you obtained any help for this homework assignment other than the text and class notes/discussion. Please give a word or two as to the nature of the help (e.g.: discussed problems, copied verbatim, whatever). Acknowledging source of help is a requirement for this assignment, and for all assignments in CSE464. It has no effect on your grade.

1. For a transmission line with Vs a one volt step at t=0, Rs, and Rt termination resistors, and Zo=100 Ohms find Vl (receiving end voltage) for the following resistor values and t<=6(l/v). Draw the waveforms for Vl. If any configurations have the same waveform draw only once and indicate which configurations it applies to.

Configuration	Rs	Rt
A	100	10^12
B	0	100
C	90	10^12
D	0	90
E	100/1.1	10^12
F	0	110
G	10	110
H	100/1.1	1000
I	100/0.9	10^12
J	0	100/0.9

2. Sketch the waveform at the input and output of a transmission line for a series terminated (sending end) transmission line with Rs=Zo, Rt=infinity, and a source voltage generating a 1V pulse of width equal to 1/2 the transmission line one-way delay l/(2v).

3. Repeat problem 2 for a square-wave voltage source which alternates between 0V and 1V with the time at each level equal to the round-trip delay 2(l/v) of the transmission line. *You should be surprised at the waveforms (at least at sending end) for this problem.*

4. A transmission line with Zo of 100 Ohms +/-10% is driven with a 0V to 1V source with output resistance (Rs) of 10 Ohms. The receiving end has a resistance to ground of Rt +/-10%. What is the maximum and minimum allowed nominal value of Rt in order for the receiving end voltage to remain at or above 0.8V after the incident wave from the 0V to 1V source transition? Put another way, 0.2V of noise (reduction in Vhigh) is to be allowed. Note that for one case (max or min resistance) the initial wave will be the limiting condition, and for the other case the first reflected wave (after three times the one-way delay) will the limiting condition

5. Use HSPICE to simulate a simple transmission-line circuit. Link to a starter .sp file is given under homework assignments. Confirm the resistor values found in problem 4 for steady state values. Note that the capacitance at the receiving end

produces spikes in the waveform that may give invalid levels for short intervals. This is one disadvantage of terminating at the receiving end when capacitance to ground is present at the receiver (it always is, capacitance is part of the receiver input). The spikes would increase in magnitude if Ct was increased or the rise/fall time was decreased. Increasing rise/fall time would decrease the amplitude of the spikes.

6. Design problem: You have been assigned the task of designing an interconnection from an oscillator (Vdd1=3.3V) to a clock driver (Vdd2=2.5V. The oscillator operates from Vdd of 3.3V +/-5% and can be modeled as a voltage source of 0V (L), or Vdd (H), both in series with a resistor with value 5 to 15 Ohms. The clock driver input is high impedance with Vil_max=0.6V and Vih_min=1.8V. Unfortunately the max input voltage to the clock driver is 2.6V, it is not allowed to connect the oscillator output directly to the clock driver input since the max input voltage will be exceeded. This limit on input voltage comes from protection diodes from input to Vdd in the clock driver that prevent damage to the device due to static electricity discharges. It is important to have good signal integrity for this connection since it's key to the entire system. The distance between the two circuits is 1 foot, and 50 Ohm +/-10% transmission line is available with 2ns/ft propagation delay, along with any resistors (ideal, no tolerance) that you may need. The clock signal is 200Mhz square wave with 500ps transitions. You may ignore resistance of the interconnecting transmission line and treat it as lossless. Design the interconnect including any termination resistors required and give the worst case waveforms at the receiver input. In keeping with this being a real design problem, it has not been debugged yet. It may be impossible to solve with given conditions.
7. (simple problem) Find the equation for characteristic impedance, Zo, of a coaxial connection with r1 the radius of the inner conductor, r2 the radius of the outer conductor, and eps_r the relative dielectric constant. Find by using the characteristic impedance per square of 377 Ohms/sq-rt(eps_r) and integrating from r1 to r2 in the same manner as was used for resistance on a layer of a PC board.

Be thankful that problem 6 is not the other way around, with the driver powered from 2.5V, and the receiver powered from 3.3V with Vih_min=2.6V. There is no simple solution in this case. Fortunately oscillators tend to be older technology and operate from the same or higher Vdd than other circuits.