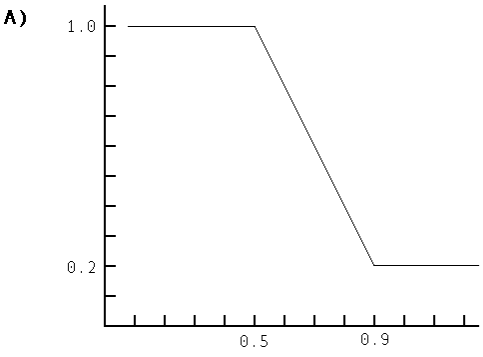
CSE464, Spring 2004, Homework #1, Due 2005.02.02, 4:00PM

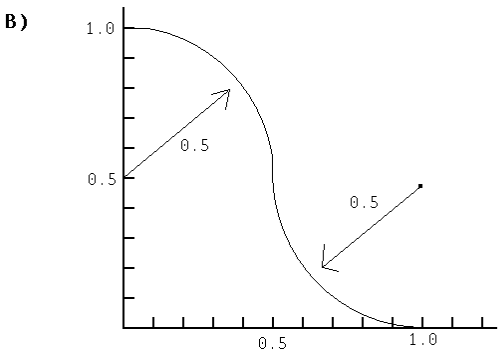
Important: Please list at top of first sheet of homework submission anyone or anything from which you obtained any help for this homework assignment other than the text and class notes/discussion. Please give a word or two as to the nature of the help (e.g.: discussed problems, copied verbatim, whatever). Acknowledging source of help is a requirement for this assignment, and for all assignments in CSE464. It has no effect on your grade unless you forget to do it.

1. Find the high and low input and output voltages, noise margins, and V_M/Vswing for each of the four transfer characteristics A), through D), shown below. V_M is the smaller of V_{ML} and V_{MH}. Vswing is the difference between high and low output level.
2. In your role as chief flunky for WWPB (World-Wide Pinball Machine) you are to summarize the DC noise margin characteristics of the SN74LVC1G08 AND gate (or circuits with its characteristics). It will be used with all four combinations of driver and receiver at nominal 2.5V or 1.8V and with all four combinations of nominal 1.8V and 2.5V at max and min value (+/-10%). Consider worst case conditions (max or min Vdd). Note: Vdd and Vcc both refer to power supply voltage, Vcc is from BJT devices, many newer data sheets refer to Vdd for MOSFETS, but not TI). Take output voltages at 100uA load. Arrange your results in a table for easy reference. Indicate which connections should be allowed, and which should not (e.g. not allowed if noise margin is less than or equal to zero). This is a very practical problem since present day logic circuits (memories, DSPs, ASICS, etc) frequently need interfacing to other circuits with differing Vdd value(s). Logic circuits are presently available for operation at 5V, 3.3V. 2.5V, 1.8V, 1.5V, 1.2V and soon we will have them at 1.0V and 0.8V. To simplify the problem a little, while not deviating too much from real specs, take Vih=0.65*Vcc and Vil=0.35Vcc for all Vcc,

   As an example of one case, for a High level and nominal Vdd of 2.5, the worst case would be driver at 2.5V minus 10% (2.25V) and the receiver at 2.5V plus 10% (2.75V). Please give answers in order H level, then L level, for the 2.5-2.5, 2.5-1.8, 1.8-2.5, 1.8-1.8 volt combinations with 0% power supply tolerance first, +/-10% power supply tolerance second. A spreadsheet (e.g. Excel) is recommended for the calculations.
   Texas Instruments SN74LVC1G08 http://www-s.ti.com/sc/ds/sn74lvc1g08.pdf
   Just for fun, note the incredibly small package <1mm x 1.5mm available for this logic.

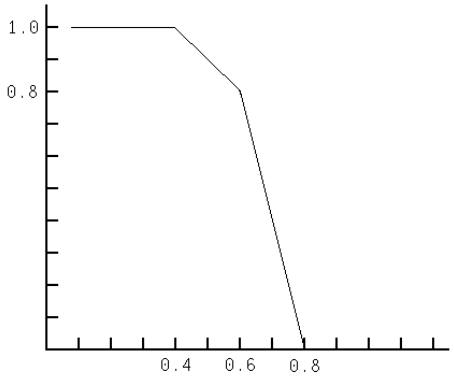
3. For the transfer Characteristic given in Figure B and the definition of noise margin given in many texts (the noise margins are taken as the difference between transfer characteristic unity gain points for inputs, and the *normal operating points for outputs (i.e.,0V and 1V),* find the voltage at each node of the circuit shown in Figure E. What conclusion can you



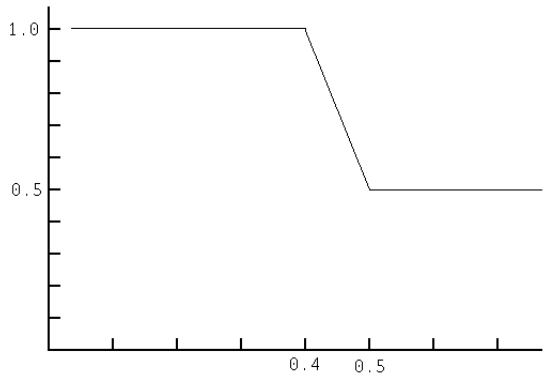


   draw from this?
4. Repeat the previous problem with the definition of noise margin given in class (Max Square) and compare the results with problem 3.

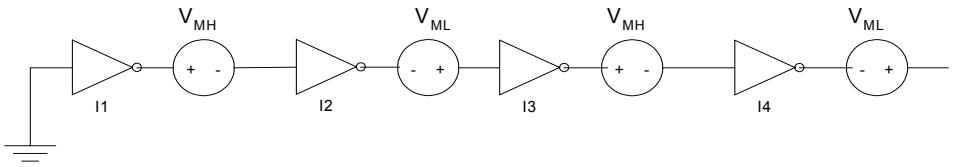
C)



D)



E) Four inverters with noise sources



5. Simulate a simple RC circuit with HSPICE and compare simulated results to pencil-paper calculation. A .sp file which can be used for this simulation is available under Jan 26 Lecture Note Pointers. *Remember*, the answer is not the simulation result, but your interpretation of it. Less than half credit for completing the simulation and supplying results with no explanation or comment. What did you learn from the simulation????!!!! HSPICE is available on the PCs in Urbauer 116 and the CEC systems. Your ID card should unlock the door. You need the login and password (given in class, or ask by e-mail), and after logging in with that, you can login to your cec account and use your disc partition there. You may use a different SPICE available where you work or other, but I recommend against it. HSPICE is the industrial-strength standard. It has capabilities well beyond others (e.g., PSPICE).

6. CSE564 Only: Comment on the calculation of noise margin for CMOS inverters in "Principles of CMOS VLSI Design" by Weste and Eshraghian, 1985. The calculation is in the appendix, pages 506-508 (CMOS only, you may ignore the NMOS calculations). This is also given in Sedra and Smith, "Microelectronic Circuits", Fourth Edition, pg 1045-1052, which may be easier to obtain. No calculations are requested here, just a comment on the methodology.