

ANCS 2006

**ACM/IEEE Symposium on Architectures for
Networking and Communications Systems**

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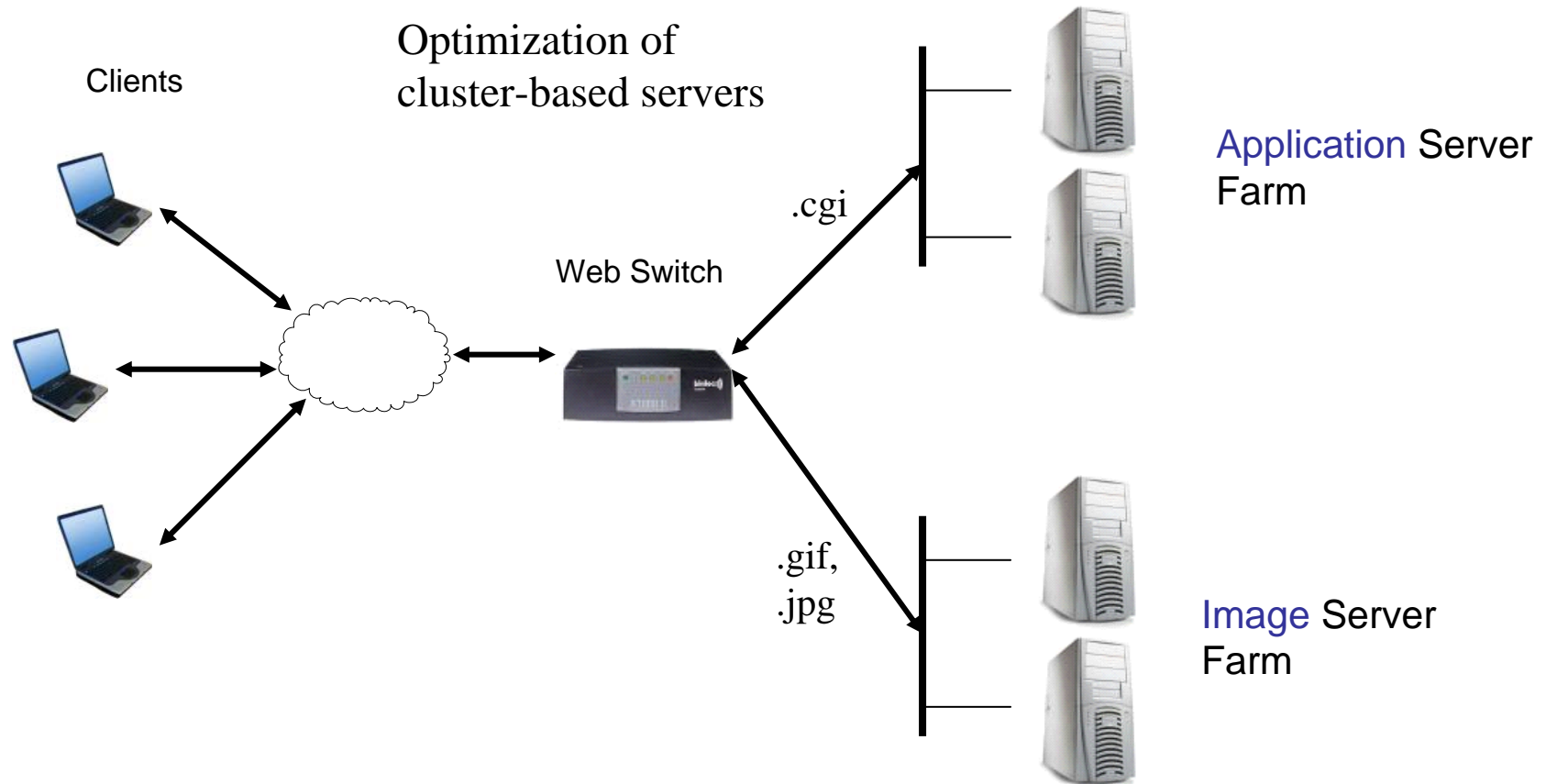
Design of a Web Switch in a Reconfigurable Platform

Christoforos Kachris

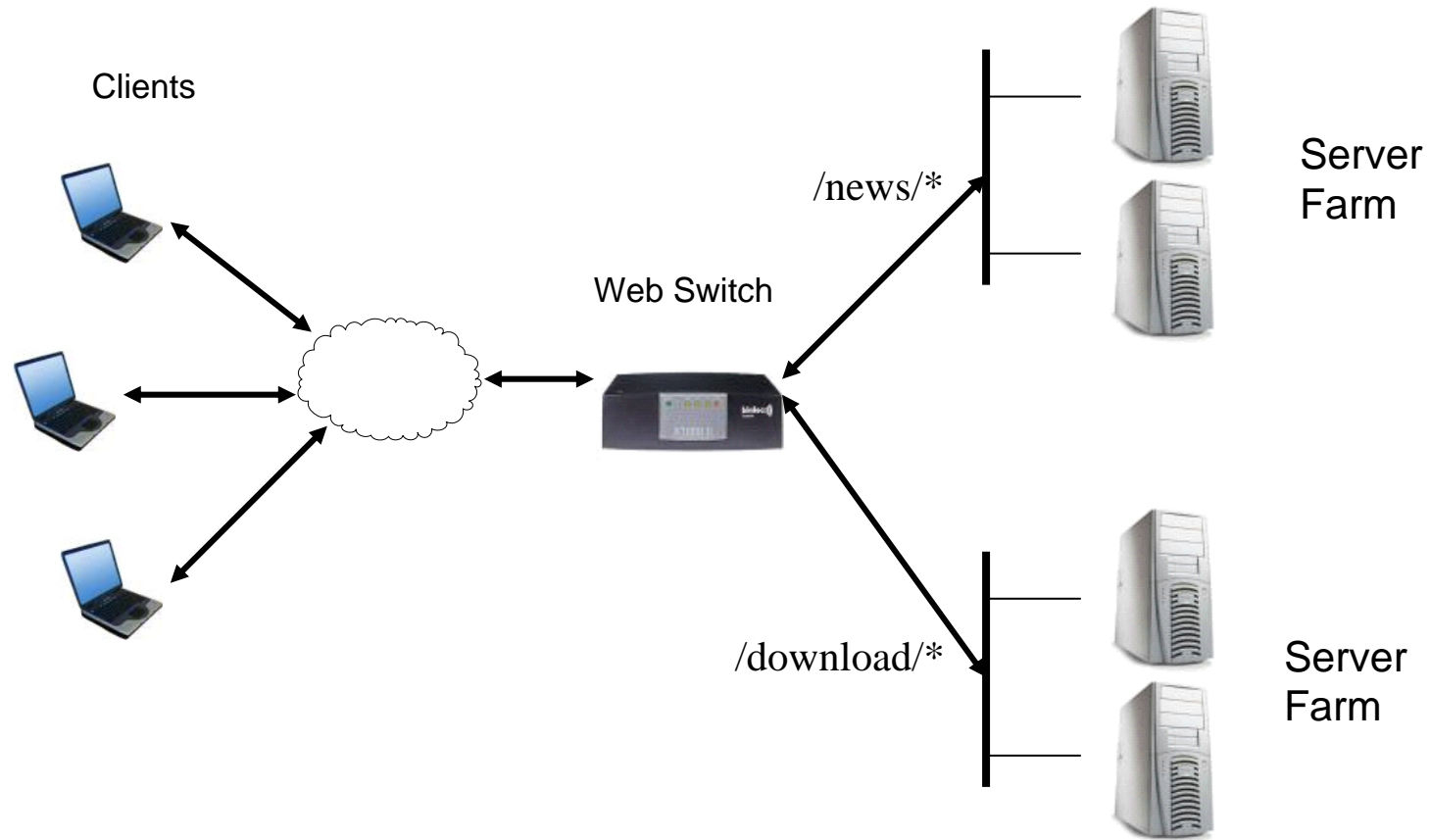
Stamatis Vassiliadis



Definition of a Web Switch



Definition of a Web Switch

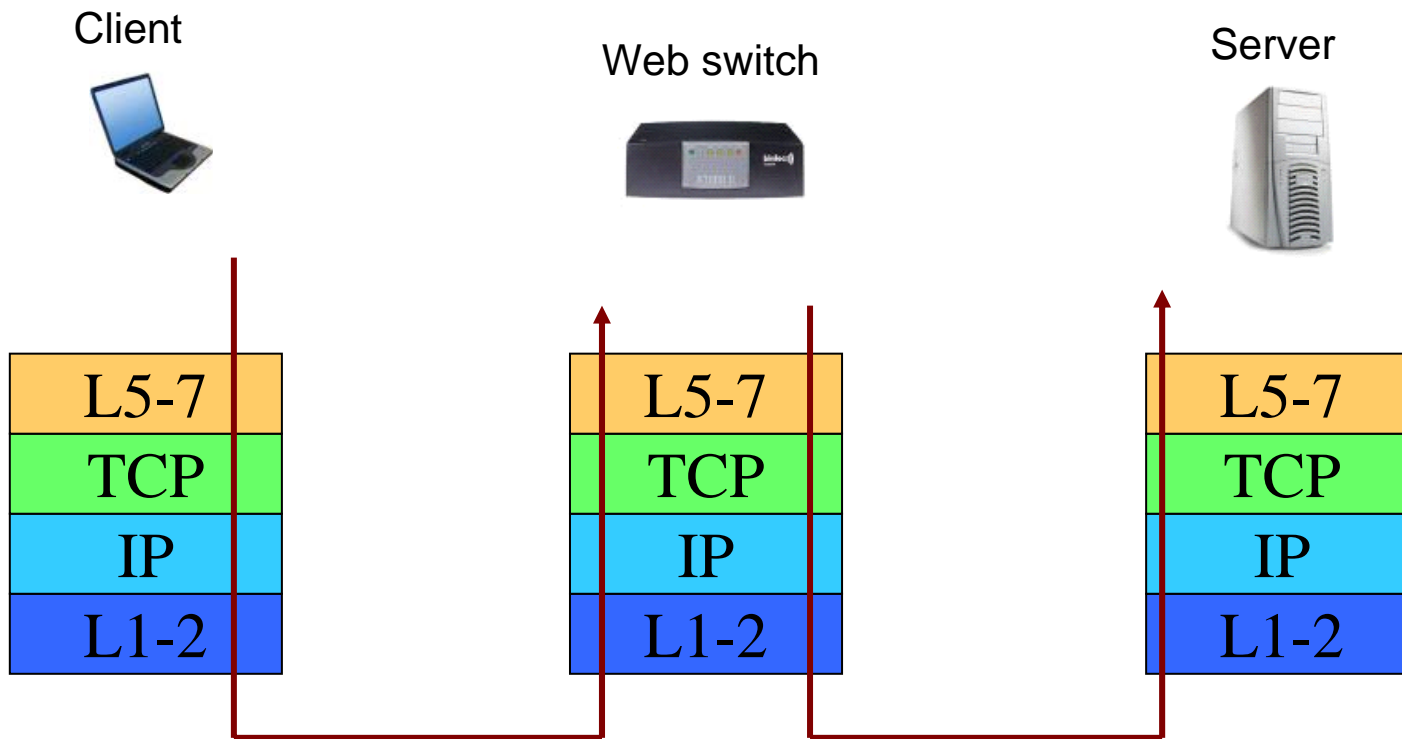


Benefits & Types of Web Switches

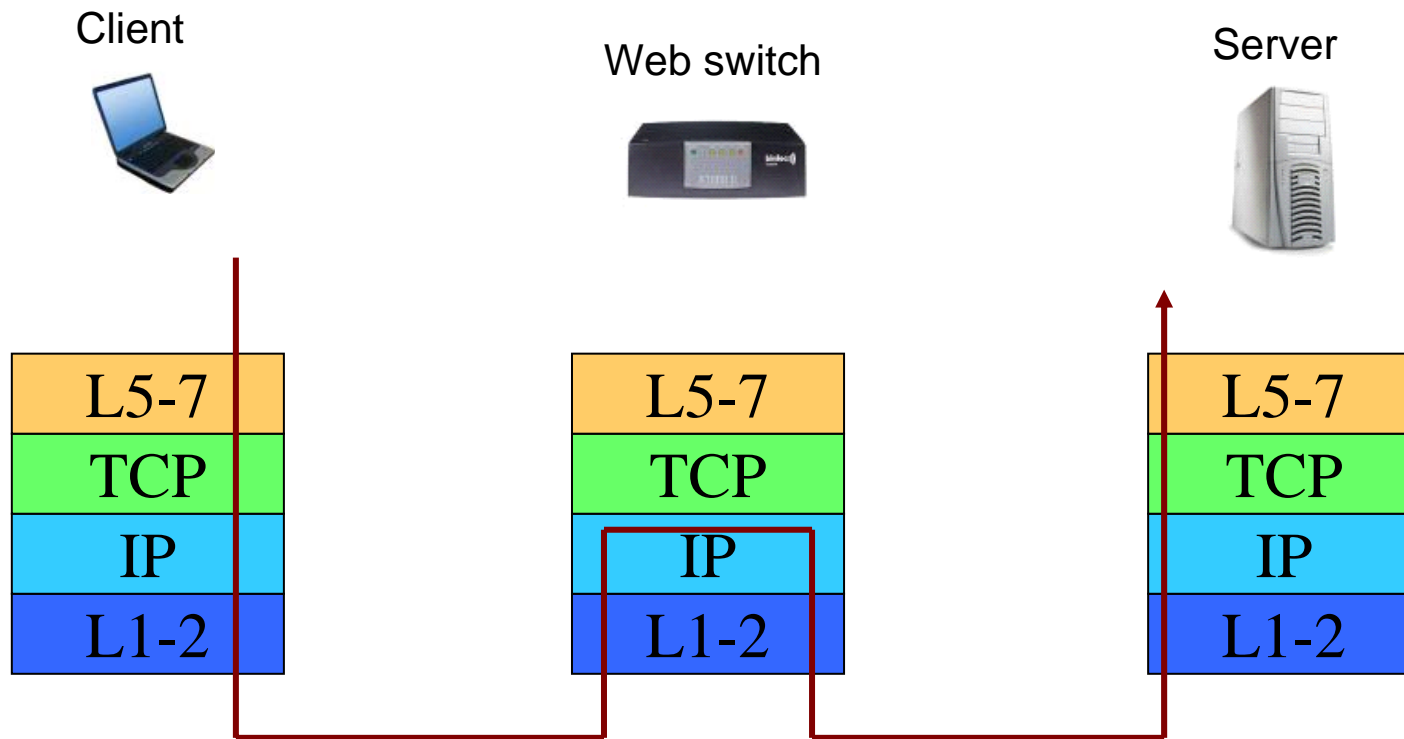
- Benefits
 - Scalability and acceleration of application
 - Persistent user session on a server
 - Content customization (e.g. regional based)
 - Faster response
- Types
 - URL-based load balancing (directory/application)
 - Cookie-based load balancing

[Source: Cisco Layer 7 Load Balancing and Content Customization]

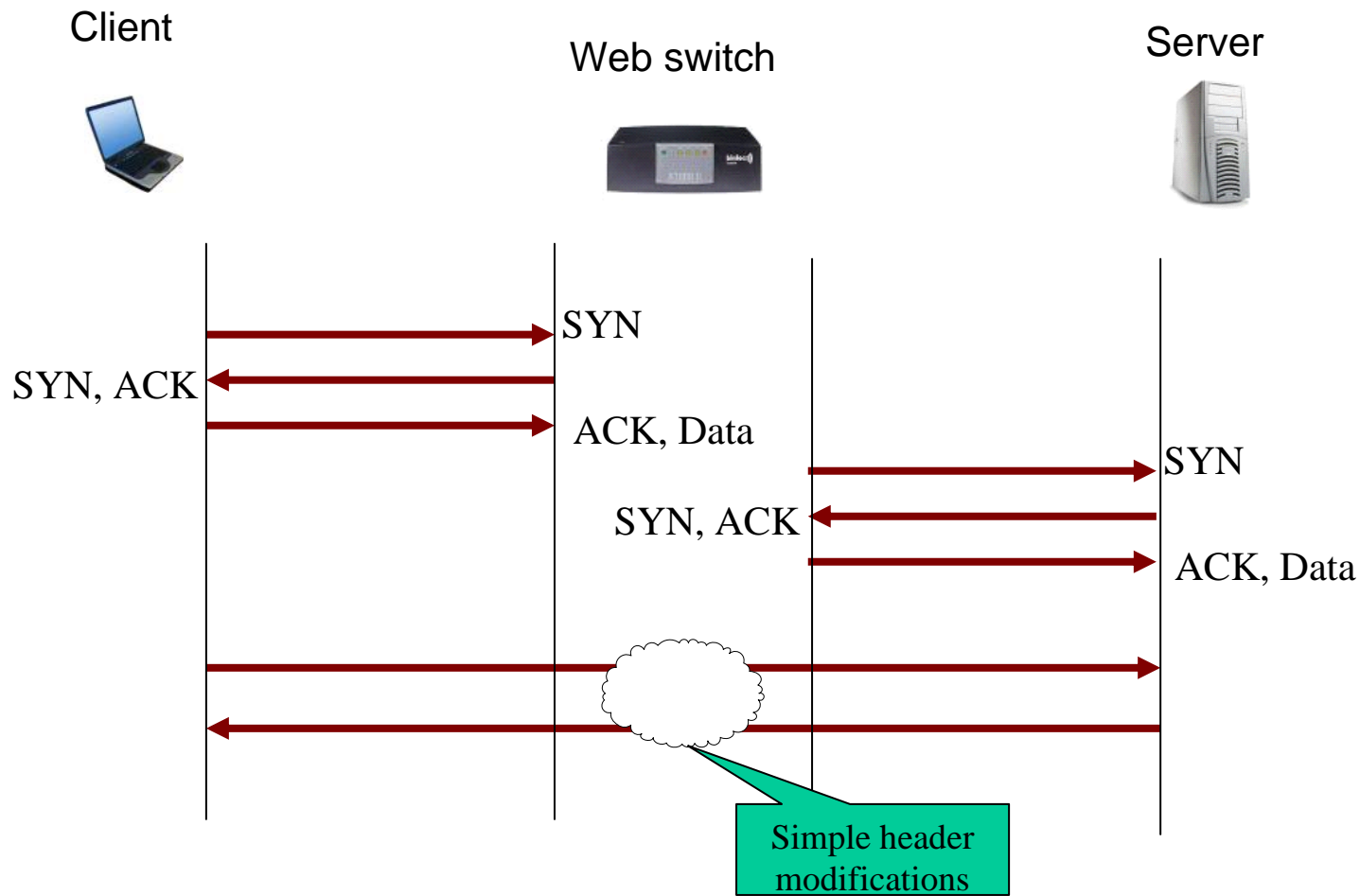
TCP Gateway



TCP Splicing



Web switch with TCP Splicing



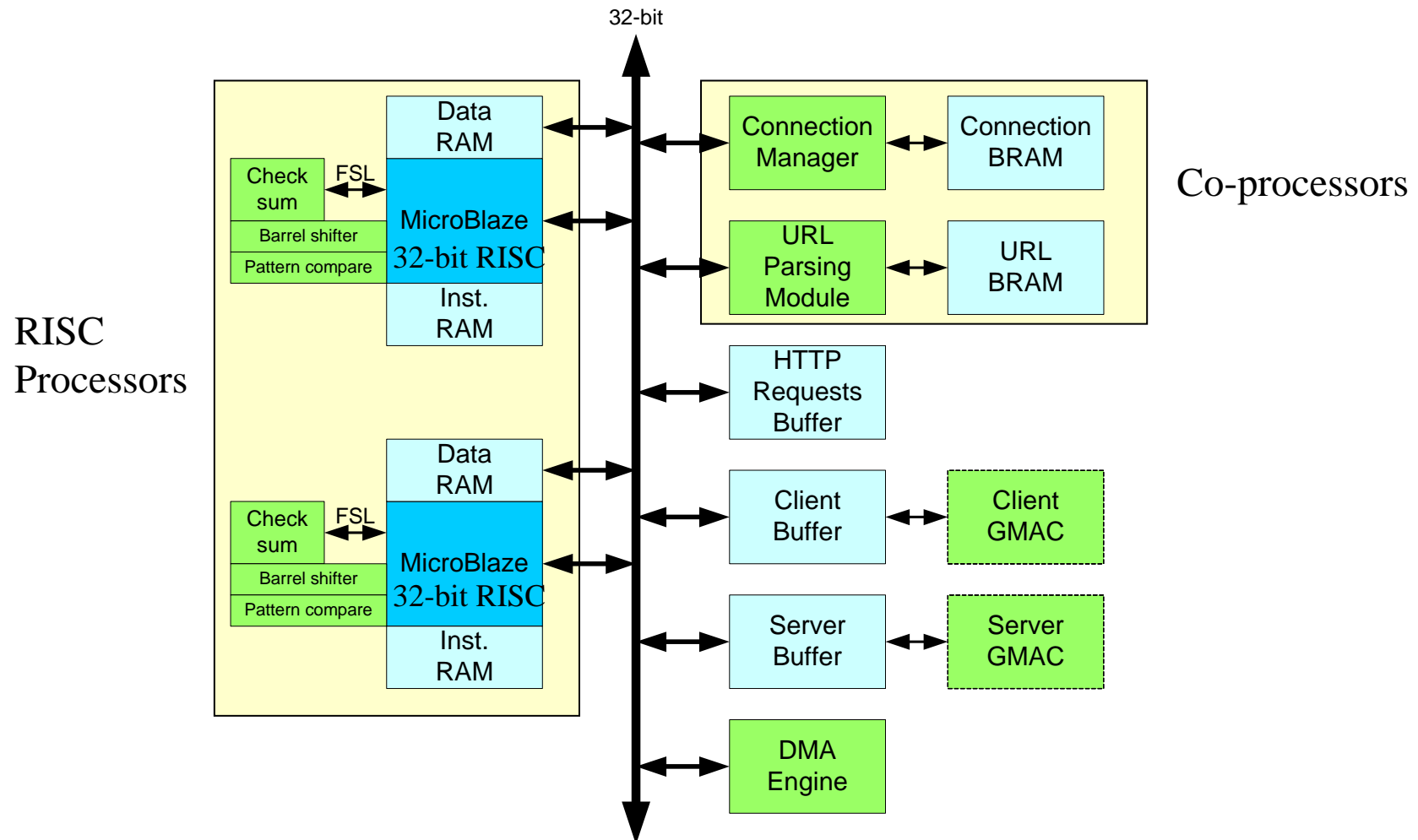
Implementation of Web Switches

- **Software** (Yang'99)
 - High flexibility 😊
 - Low performance ☹️
- **ASIC** (Apostolopoulos'00)
 - High performance 😊
 - Low flexibility ☹️
- **Network Processors** (Zhao,Bhuyan'05)
 - High performance 😊
 - High flexibility 😊
 - High power ☹️

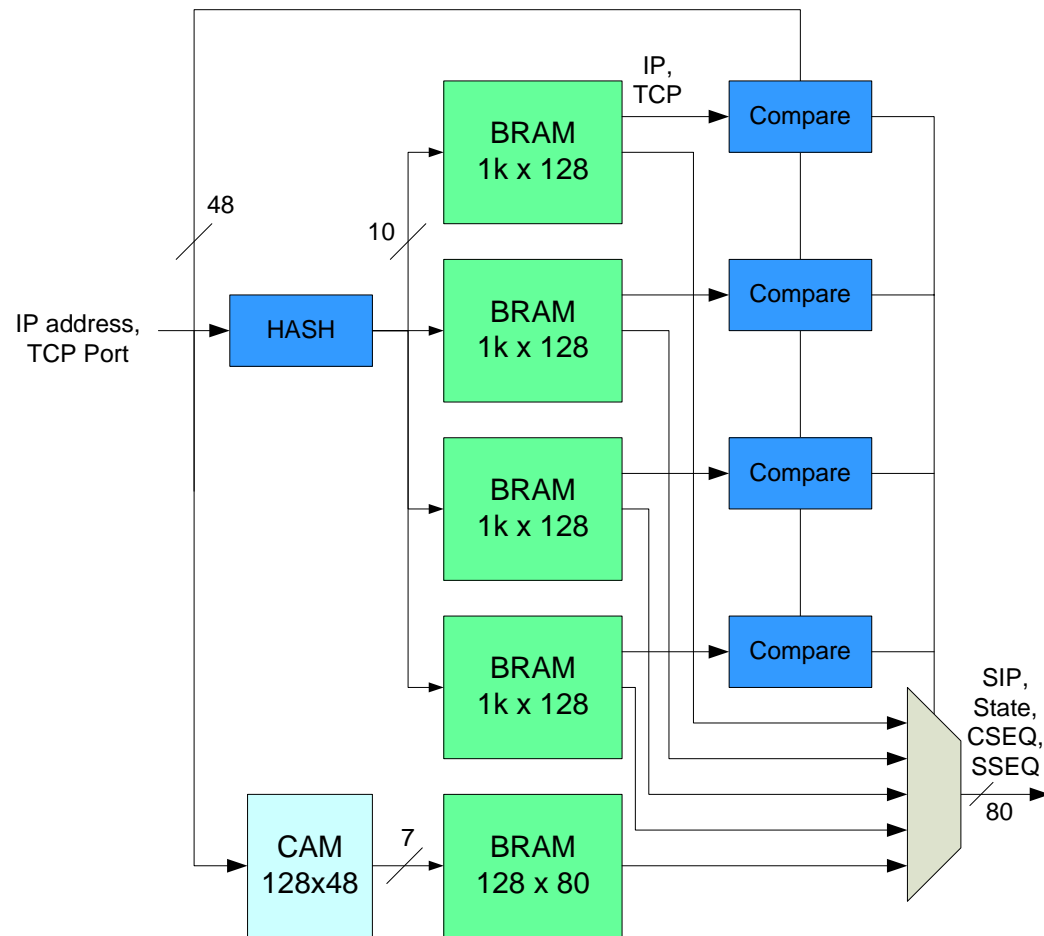
FPGA-based Web Switch

- High flexibility using RISC processors
 - Not vendor specific language
- High throughput using co-processors
 - Reconfigure co-processors based on the type of web switch
- Low Power

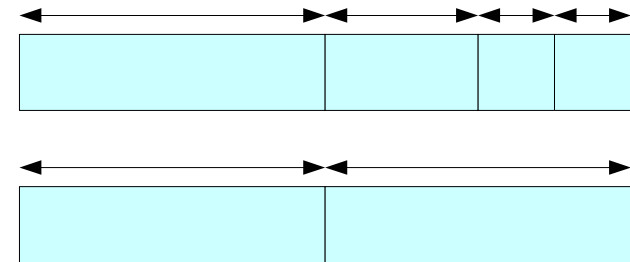
Architecture



Connection Manager



Write (IP, TCP, SIP, state, Client SEQ, Server SEQ) return 0;
Search (IP, TCP) return SIP, state, Client SEQ, Server SEQ;
Delete (IP, TCP) return 0;

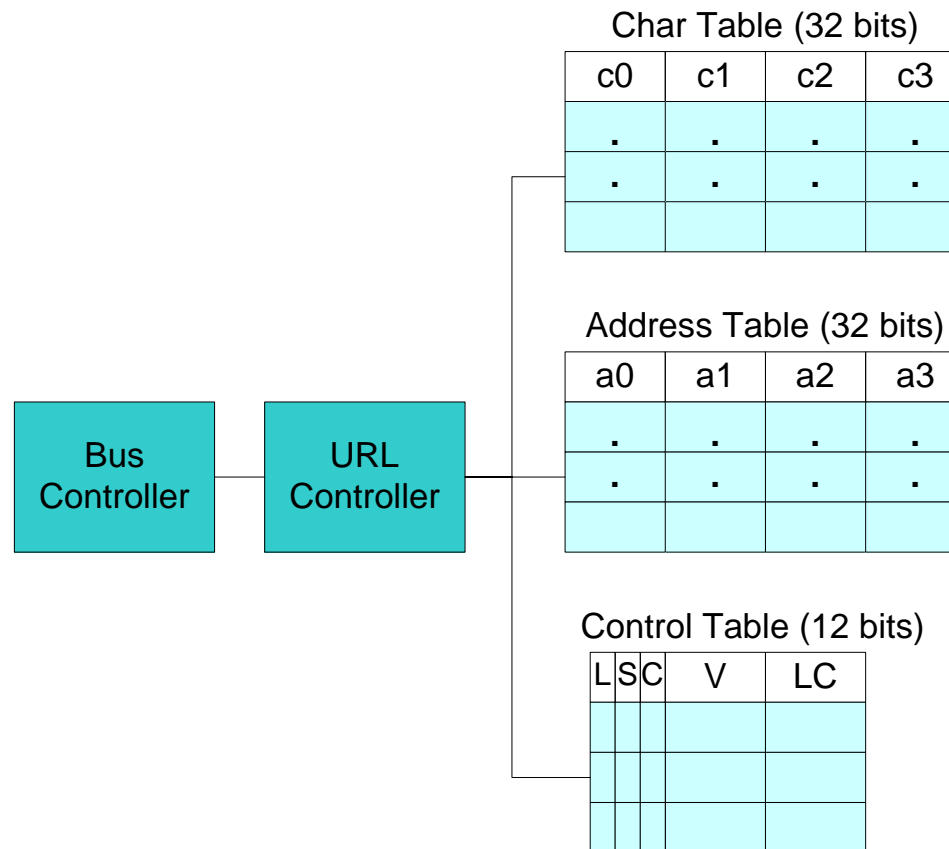


Collision probability

Number of BRAMs	Collision Probability	
	128CAM	256CAM
2	18%	15%
3	11%	8%
4	4%	1%
5	0%	0%

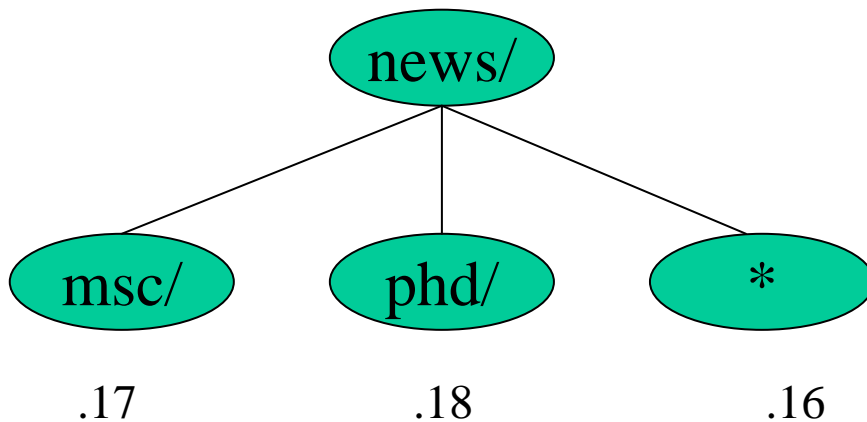
Using the UC Berkeley-home IP traces (Nov 17)

URL Parsing Co-processor



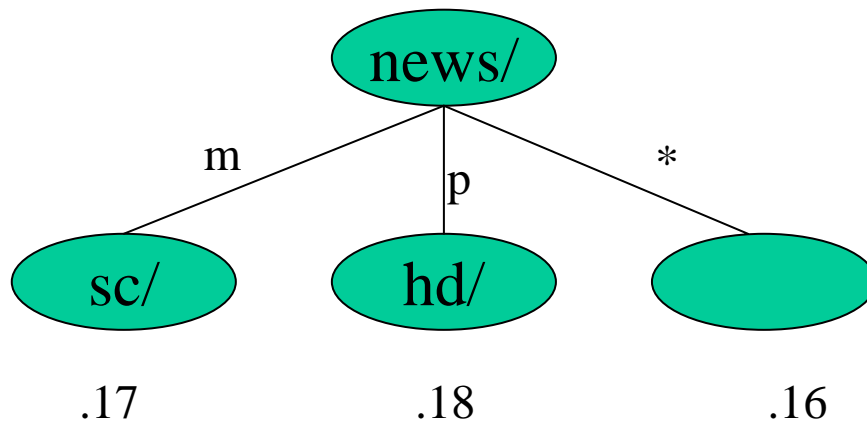
URL Co-processor example

URL	Server IP
/news/*	.16
/news/msc/	.17
/news/phd/	.18



URL Co-processor example

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Char Table

1	n	e	w	s
2	/			
3	m	p	*	
4	s	c	/	*
5	h	d	/	*

Address Table

3			
4	5	.16	
			.17
			.18

Performance of URL Co-processor

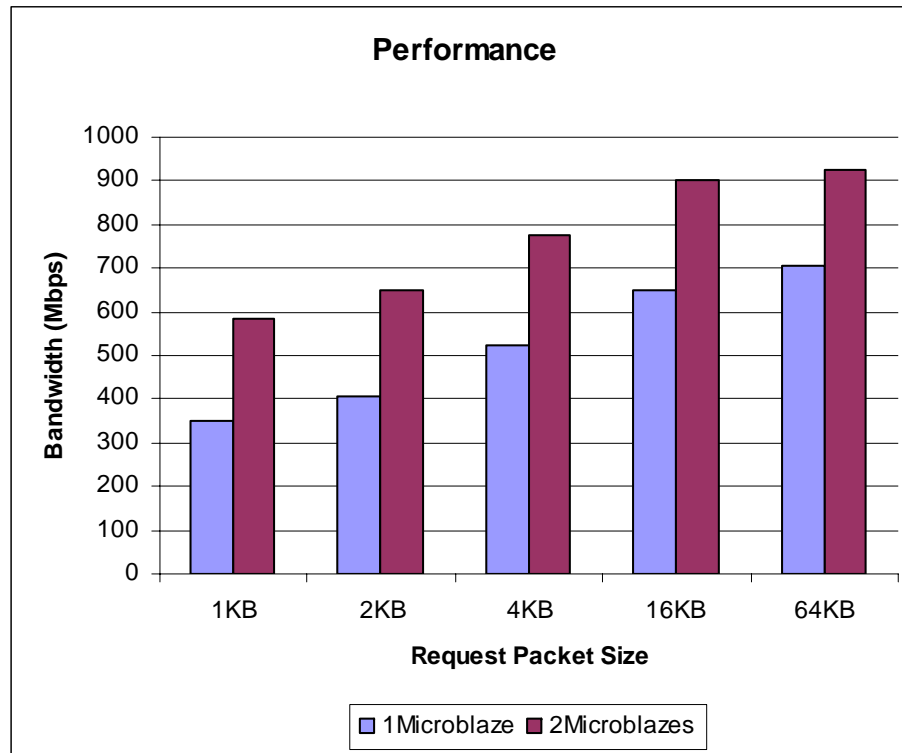
- 1-4 chars/cc
- Most of the URLs are <28 char for the first two strings of the directory (based on the San Diego Super Computing Center Web Traces (www.web-caching.com))
- ~11cc per URL

Packet Processing Latency

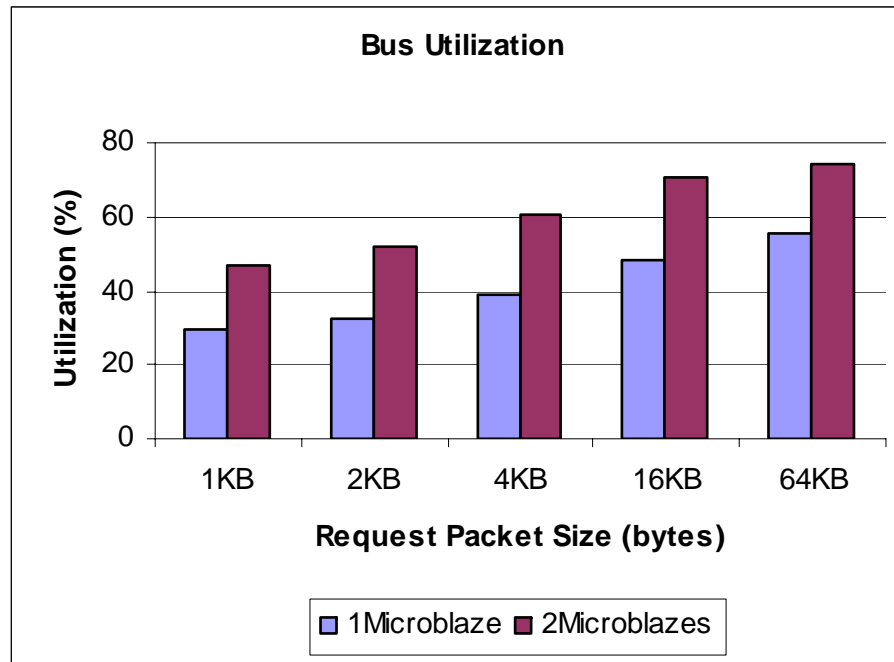
Packet Type		Latency (us)		
		Reconf.	IXP2400[3]	Linux[3]
Control Packet	SYN	5.5	7.2	48
	ACK/Req.	8.8	8.8	52
	SYN/ACK	8.5	8.5	42
Data Packet	Data	6.9	6.5	13.6
	ACK	6.6	6.5	13.6

Performance Evaluation

Sustained throughput for several Request packet sizes



Bus Utilization

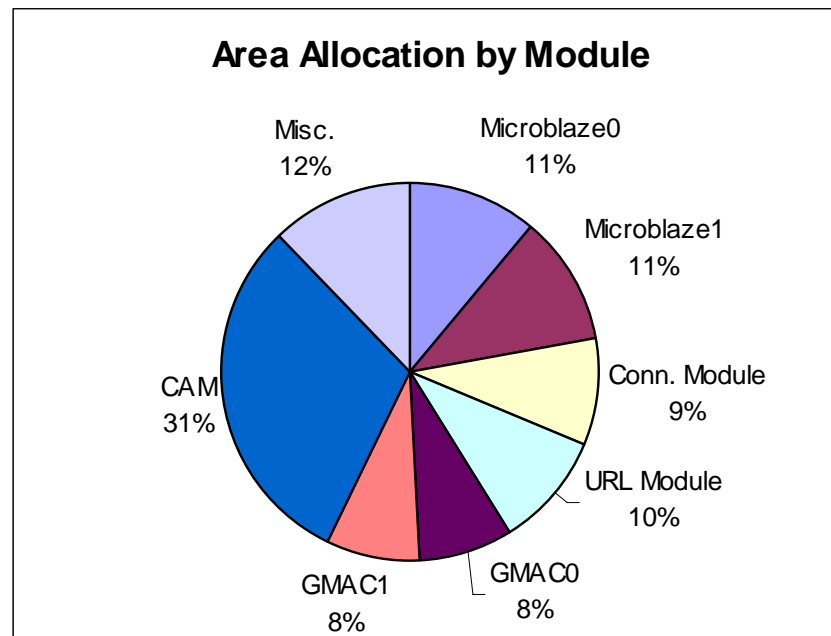


Bottleneck

- In the first case (1 processor) is the processing power
- In the second case (2 processors) the bottleneck is the bandwidth of the bus

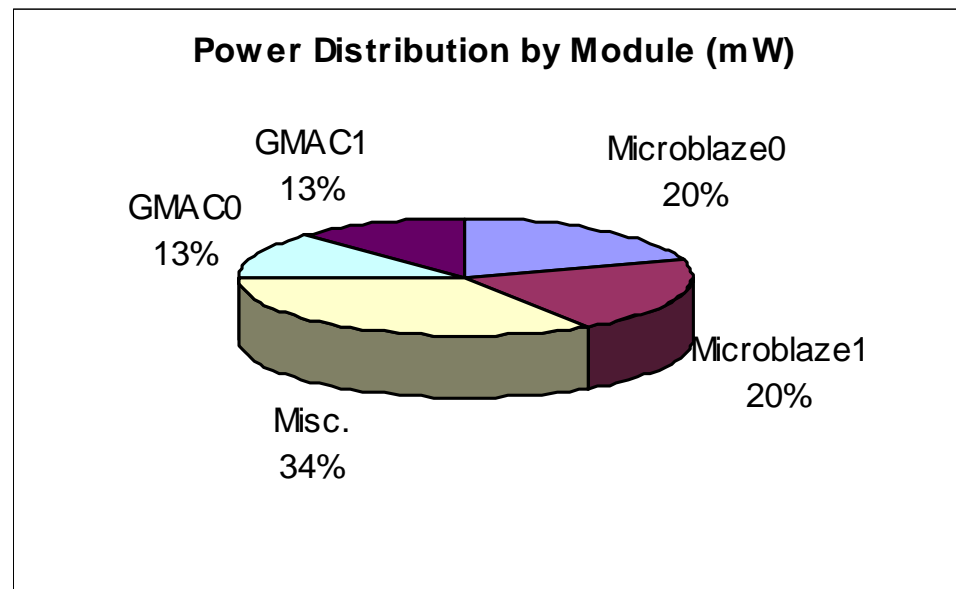
Area Allocation

- ~10000 FPGA slices in Xilinx Virtex4
(~300K gates)

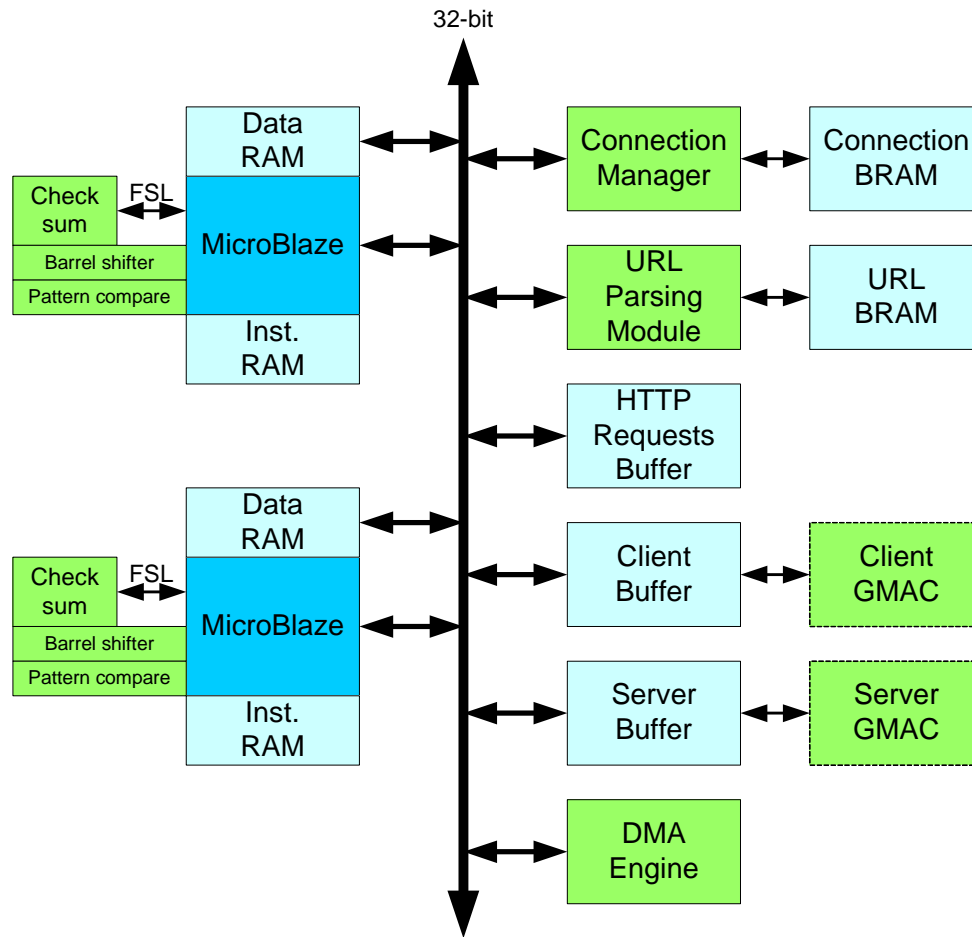


Power Evaluation

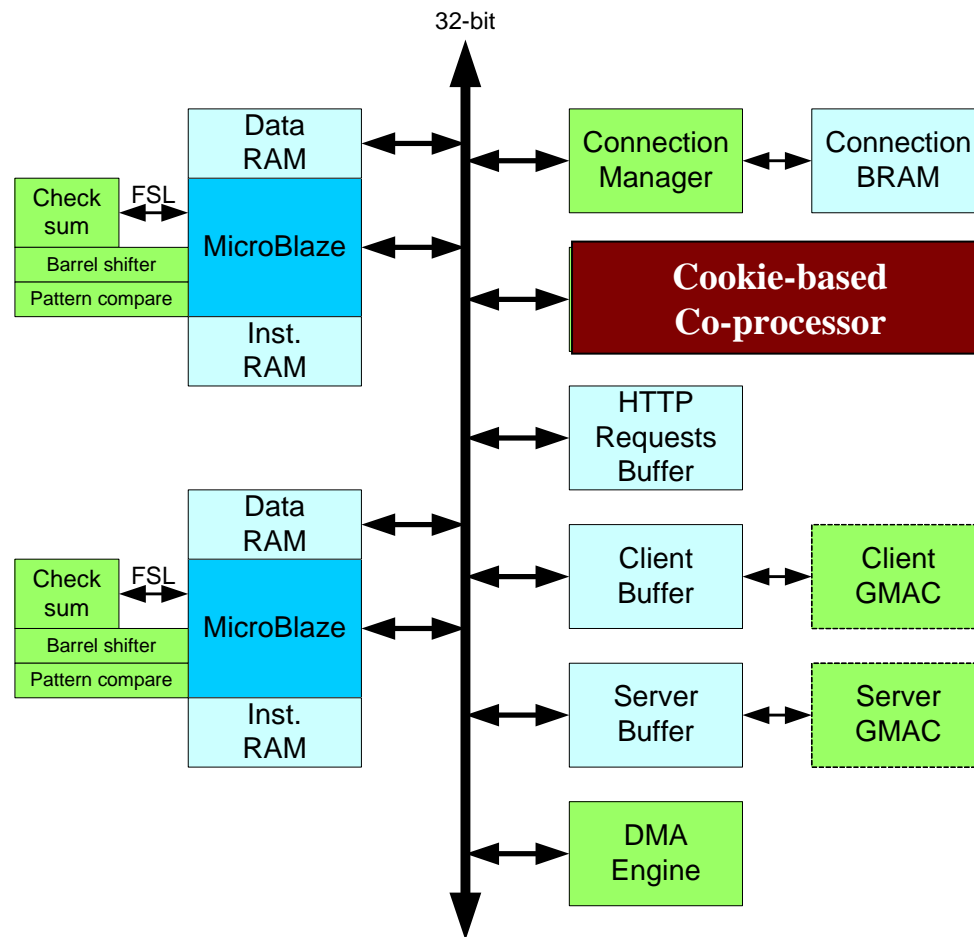
- Overall
 - FPGA based: <1W
 - NP based : ~10W



Scalability

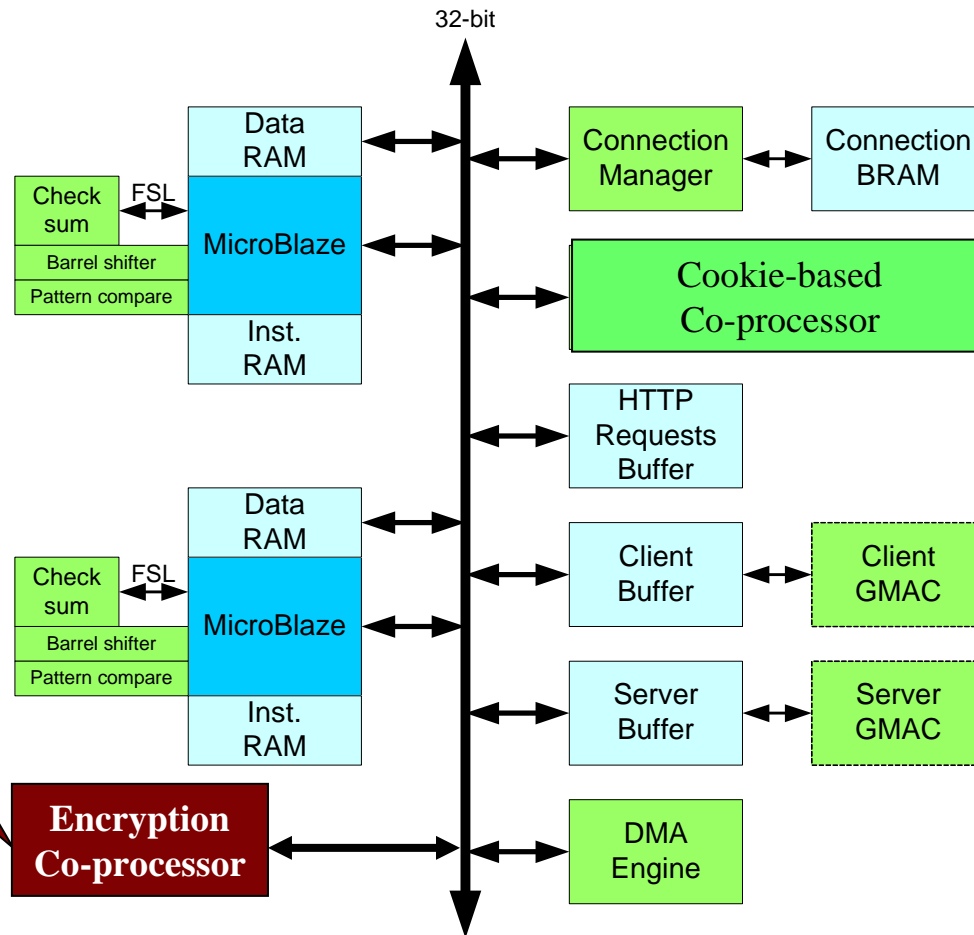


Scalability



The co-processors can be dynamically reconfigured to meet the application requirements

Scalability

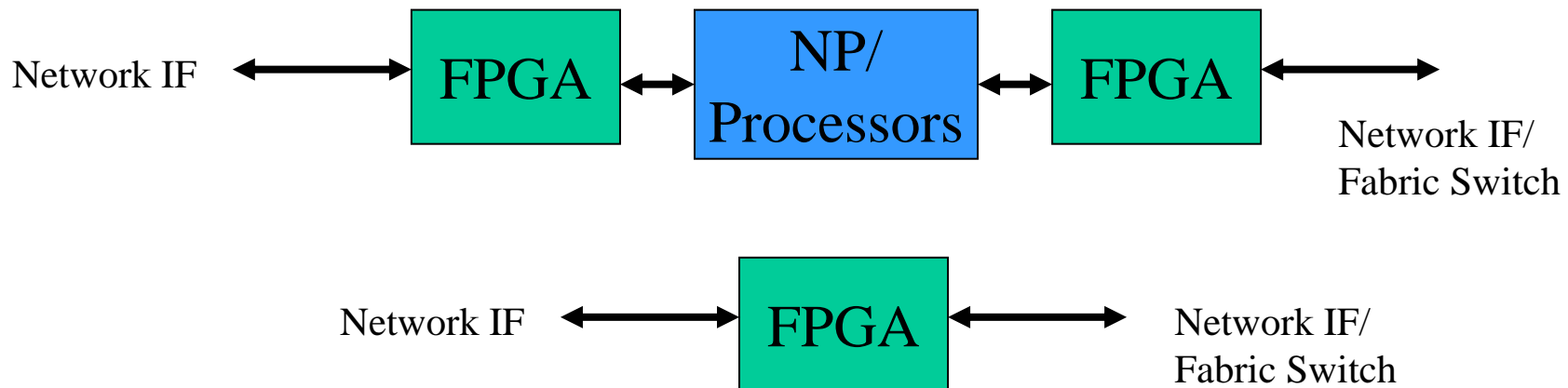


The co-processors can be dynamically reconfigured to meet the application requirements

Encryption Co-processor

Conclusions

- Until now FPGA are used for Framers/Interfaces
- Current FPGA are SoCs that can be used for the network systems (Lower cost, lower power)
 - Less \$ per packet
 - Less W per packet



Thank you!
Questions?